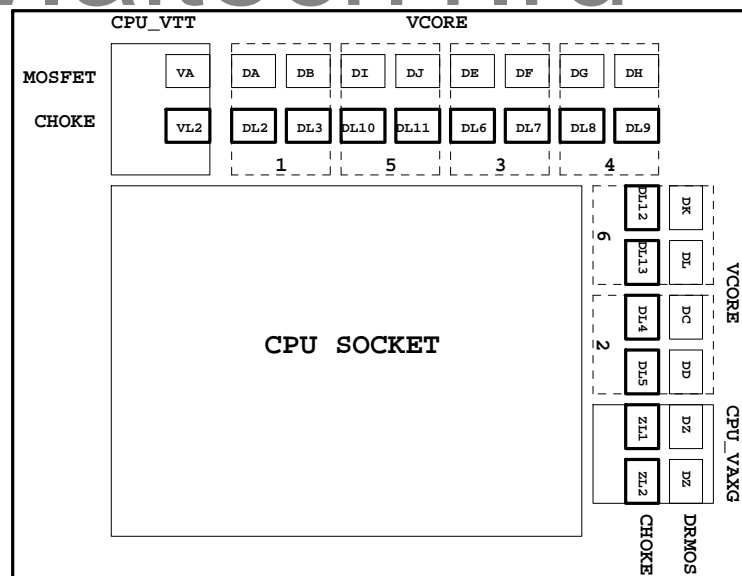


01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*16/*8/*4 SWITCH
18	PCI EXPRESS*1 SLOTS X3
19	ITE 8892
20	PCI SLOT 1
21	HDMI / DVI / DP
22	MSATA
23	Dual BIOS
24	ALC898
25	REAR AUDIO JACK
26	AMPLIFIER
27	PWM_IR 3567
28	VCORE POWER
29	VAXG POWER
30	PWM_IR 3570
31	VTT & DDR POWER
32	DISCRETE POWER I

33	VCCSA POWER
34	I/O ITE8728
35	F_PANEL , F_USB , PHOT
36	F_USB3.0
37	ATX POWER, CLOCK GEN
38	HWM,KB/MS , FAN CTRL
39	ARTHEROS AR8161/AR8151
40	INTEL 82579V
41	Marvell 9172(F+R)
42	Marvell 9172(F)
43	VT6308P 1394
44	VL810 USB3_HUB1(R)
45	VL810 USB3_HUB1(F)
46	RST, PWR, CLR_CMOS
47	TABLE LIST
48	



Gigabyte Technology

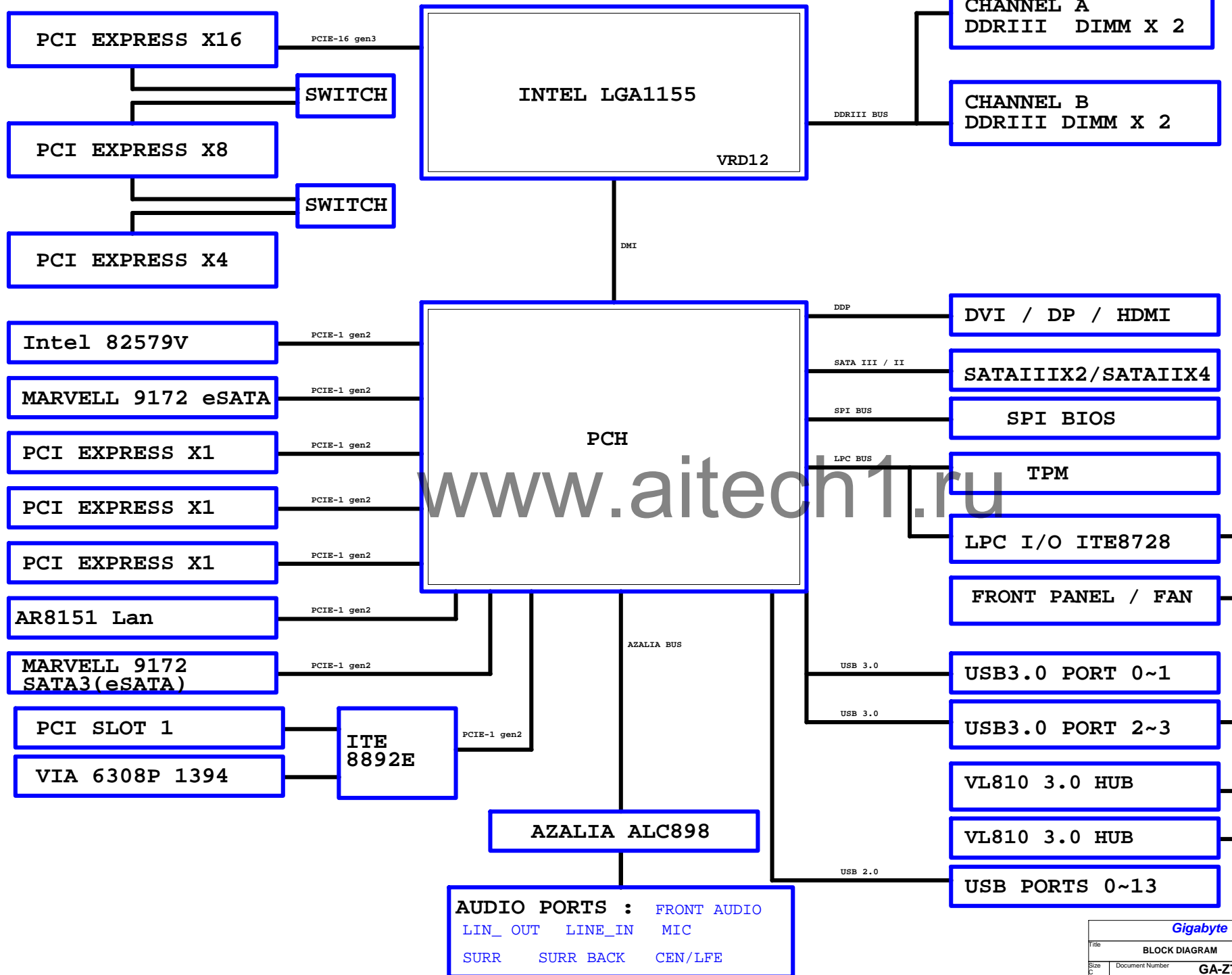
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Size	Document Number	GA-Z77X-UD5H	Rev
Custom			1.01
Date:	Friday, March 09, 2012	Sheet	1 of 47

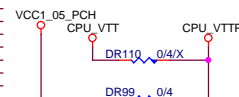
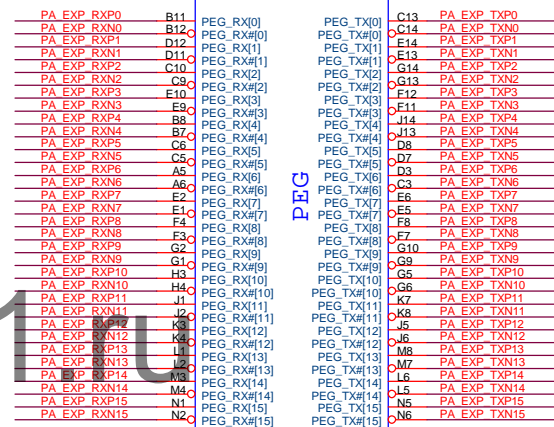
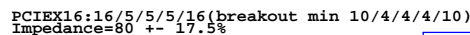
Component value change history

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[illegible]

BLOCK DIAGRAM

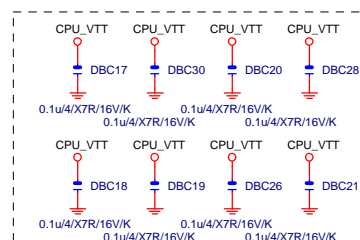
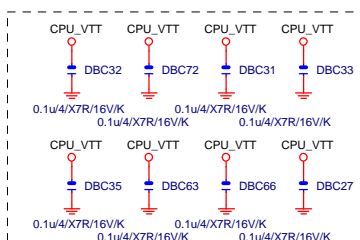
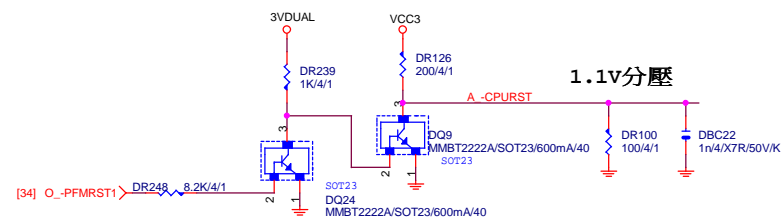
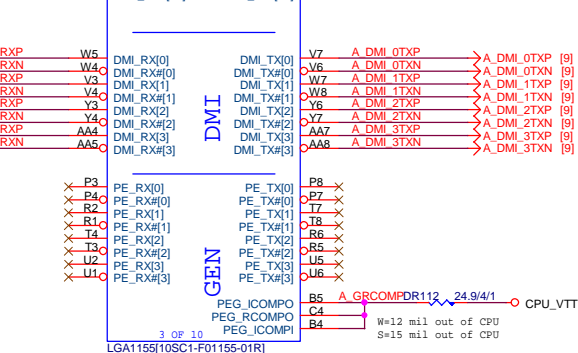
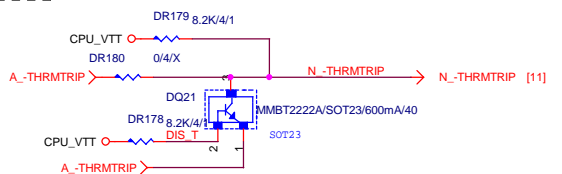
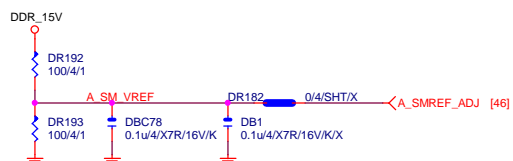
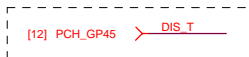




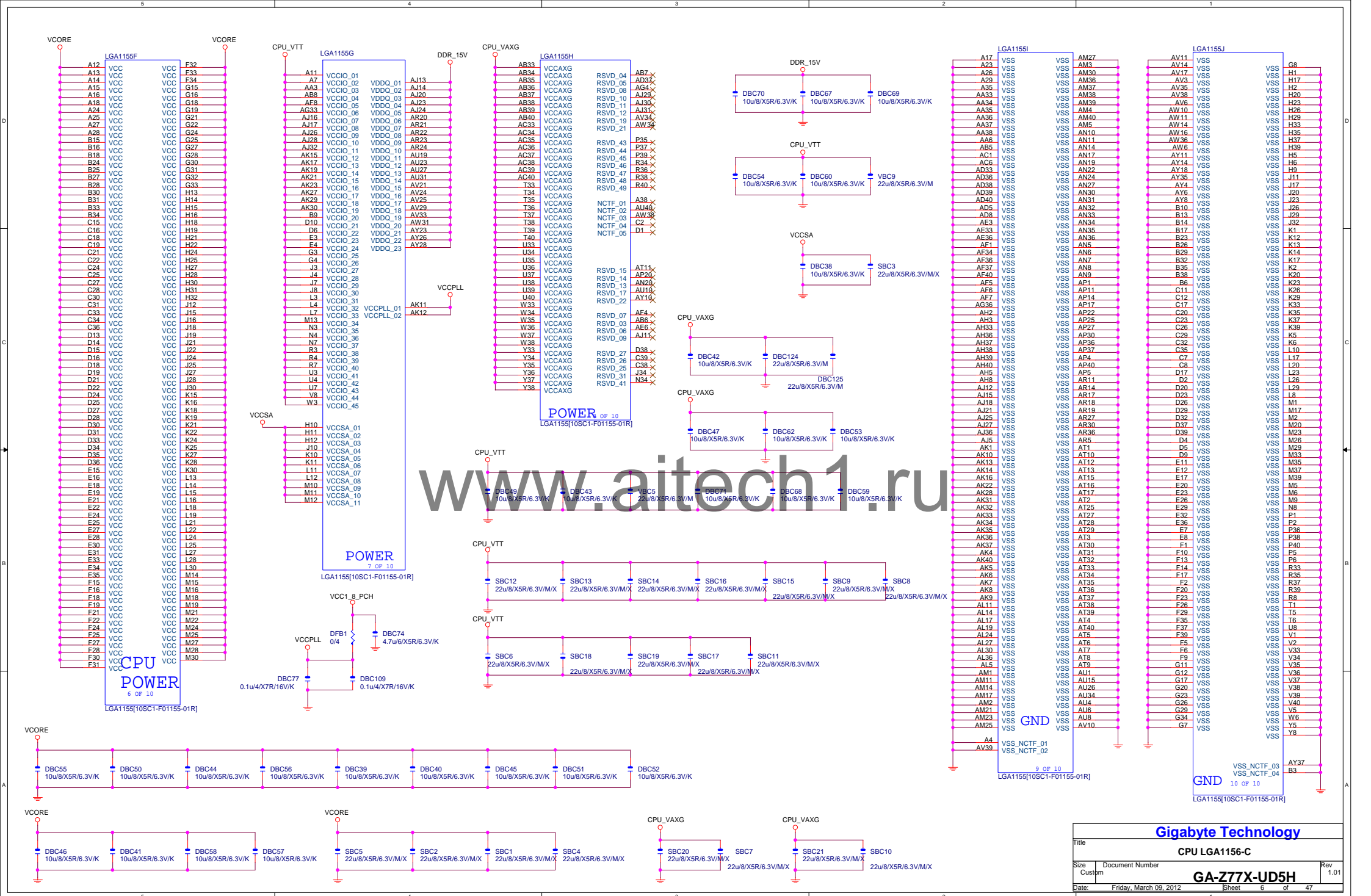
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1	0	2x8
0	1	RSVD
0	0	X8.X4.X4

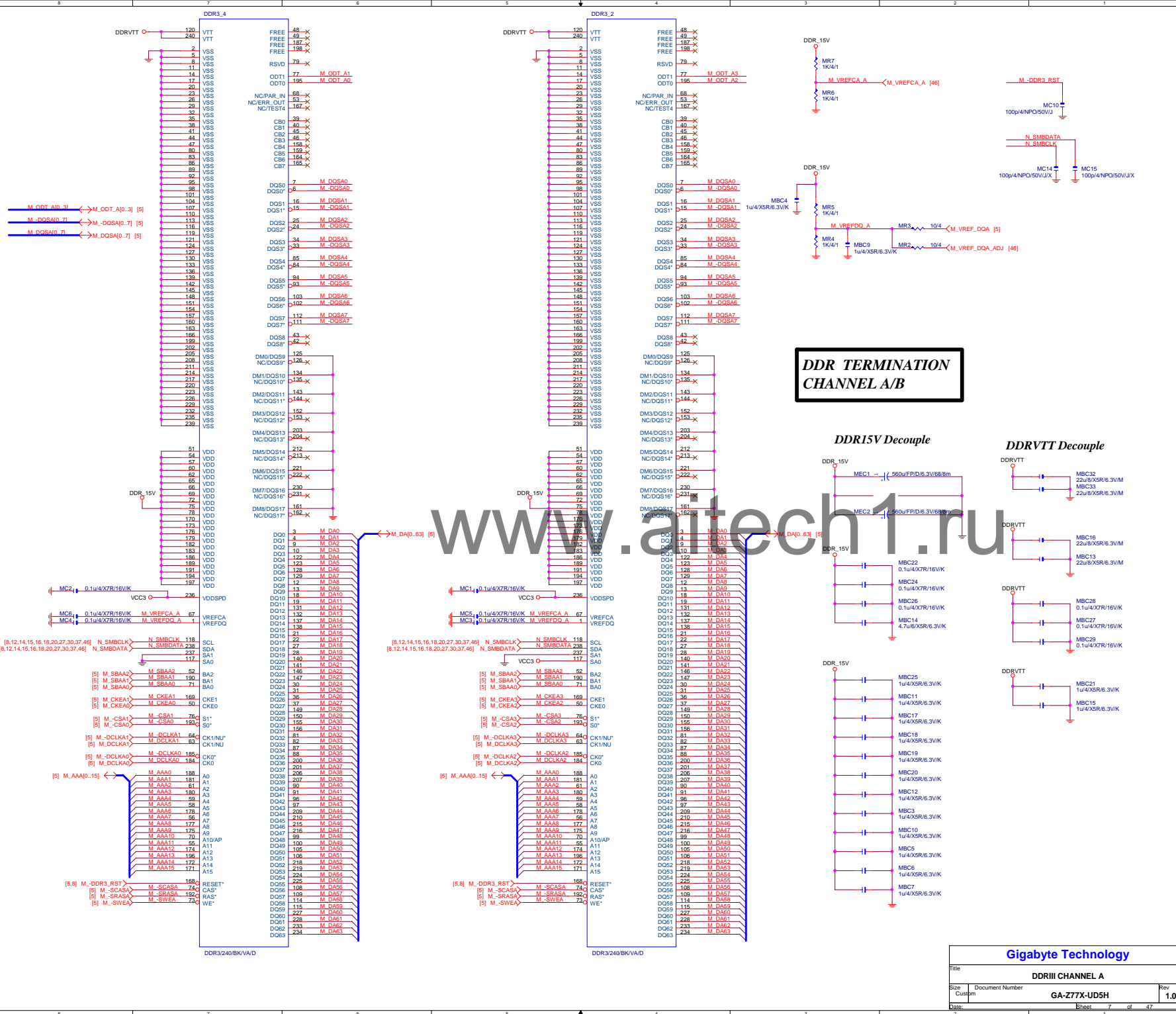
N DRAM PWROK

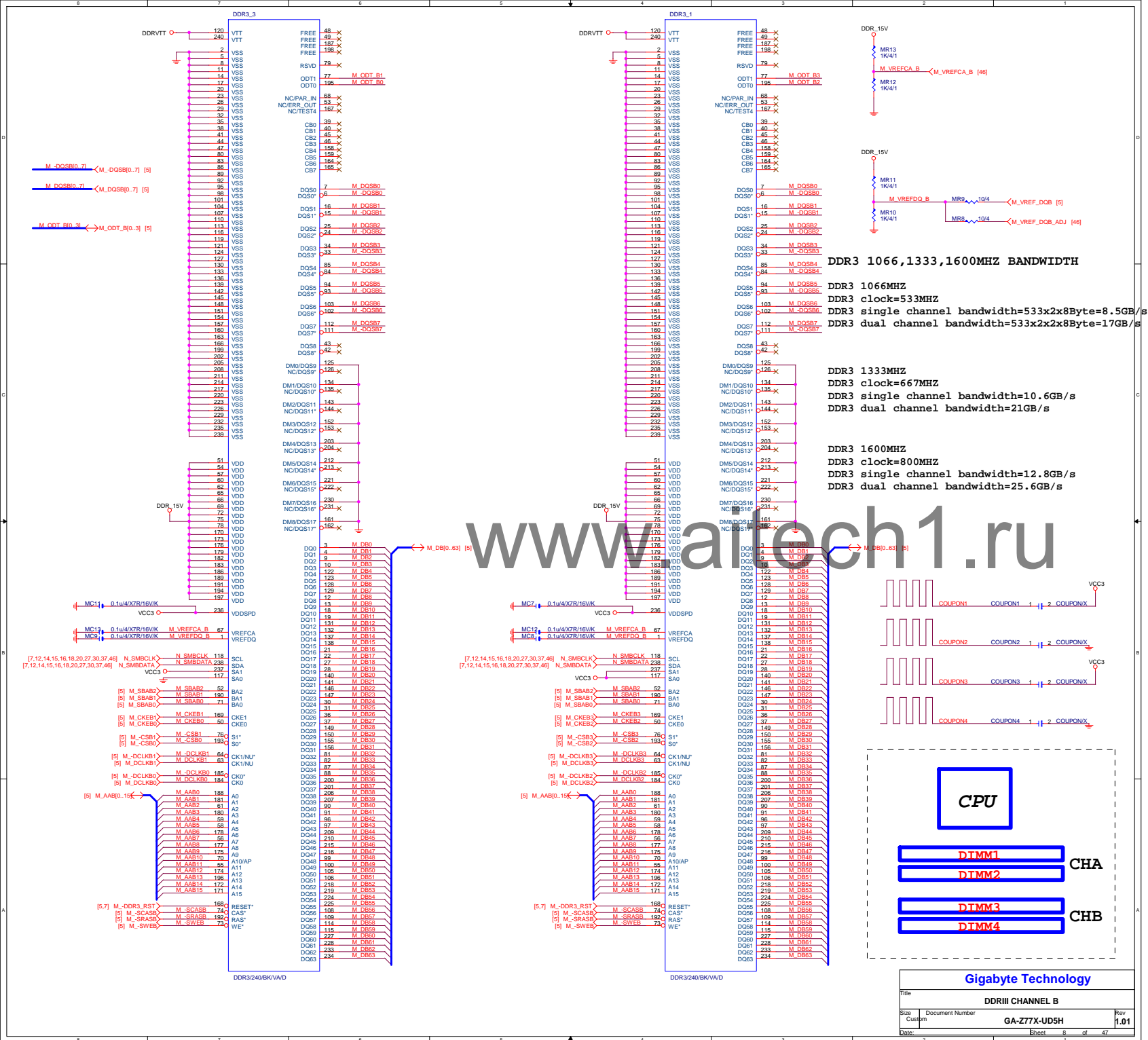
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100p/4/NPO/50V/J/X

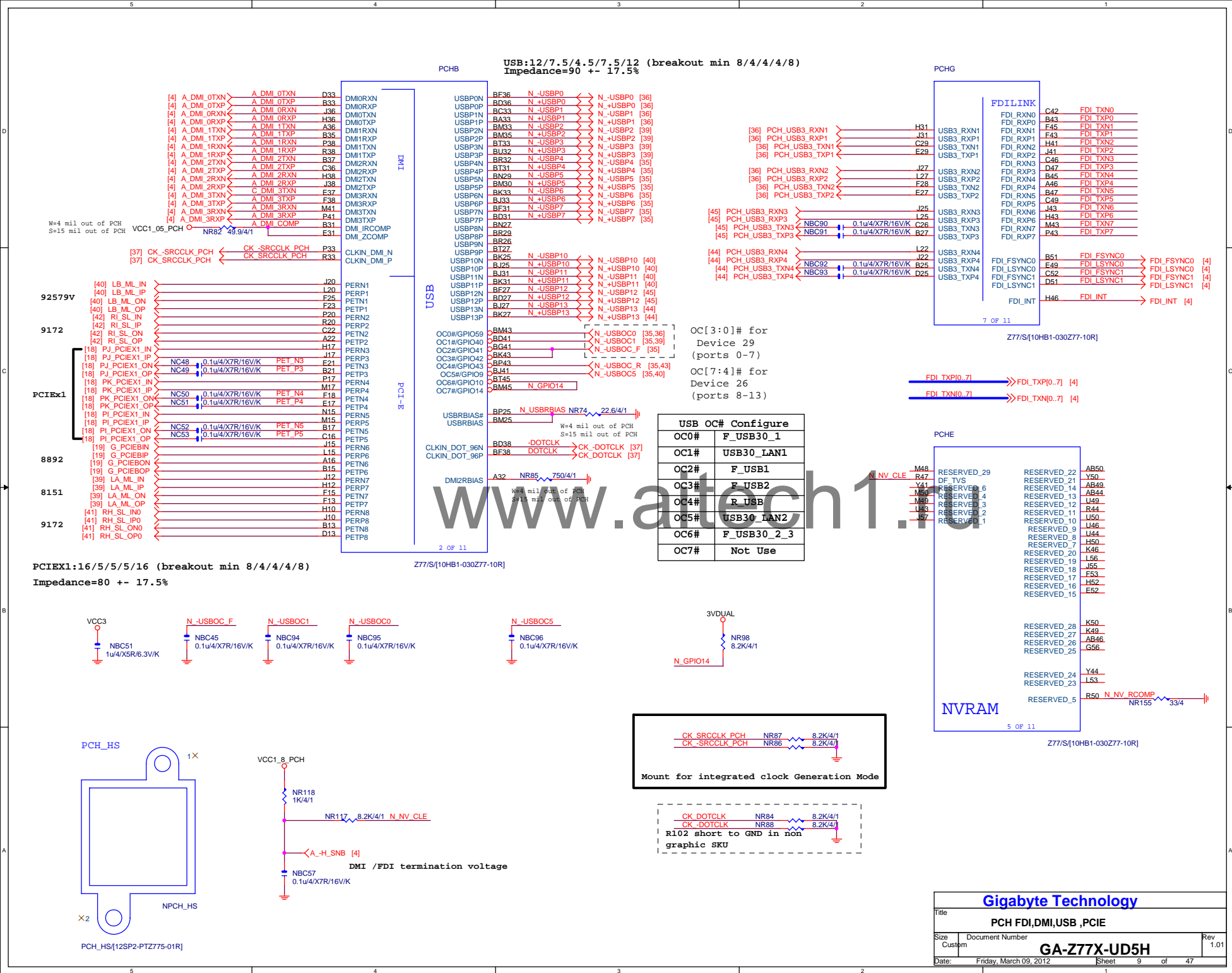


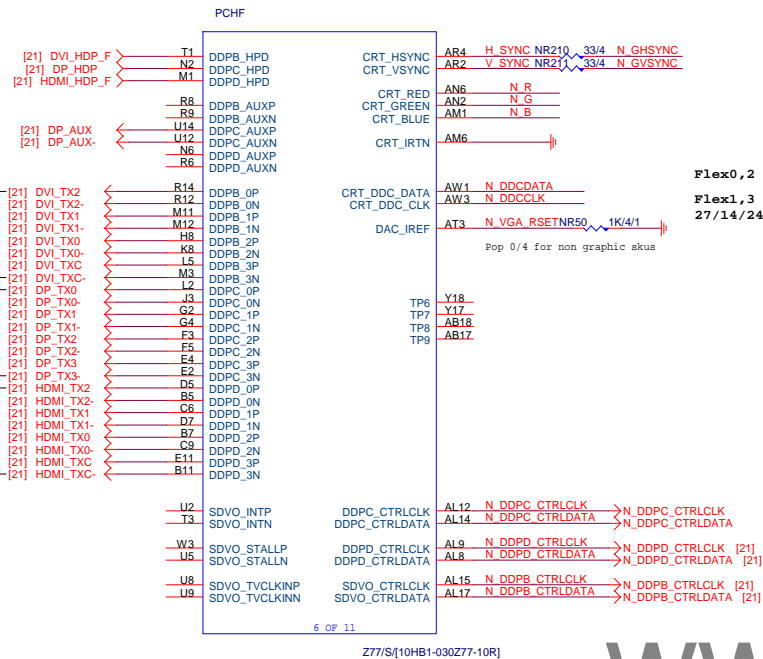
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M_AAA3	AV23	SA_MA[3]	
M_AAA4	AV23	SA_MA[4]	
M_AAA5	AT24	SA_MA[5]	
M_AAA6	AT23	SA_MA[6]	
M_AAA7	AU22	SA_MA[7]	
M_AAA8	AV22	SA_MA[8]	
M_AAA9	AT22	SA_MA[9]	
M_AAA10	AV28	SA_MA[10]	
M_AAA11	AU21	SA_MA[11]	
M_AAA12	AT21	SA_MA[12]	
M_AAA13	AW32	SA_MA[13]	
M_AAA14	AU20	SA_MA[14]	
M_AAA15	AT20	SA_MA[15]	
[7] M_SWEA	AW29	SA_WE#	
[7] M_SCASA	AV30	SA_CAS#	
[7] M_SRASA	AU28	SA_RAS#	
[7] M_SBAA0	AY29	SA_BS[0]	
[7] M_SBAA1	AW28	SA_BS[1]	
[7] M_SBAA2	AV20	SA_BS[2]	
[7] M-CSA0	AU29	SA_CS#	
[7] M-CSA1	AV32	SA_CS#	
[7] M-CSA2	AW30	SA_CS#	
[7] M-CSA3	AU33	SA_CS#	
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[7] M_CKEA2	AU18	SA_CKE[2]	
[7] M_CKEA3	AV18	SA_CKE[3]	
M_ODT_A0	AV31	SA_ODT[0]	
M_ODT_A1	AU32	SA_ODT[1]	
M_ODT_A2	AU30	SA_ODT[2]	
M_ODT_A3	AW33	SA_ODT[3]	
[7] M_DCLKA0	AY25	SA_CK[0]	
[7] M_DCLKA0	AW25	SA_CK[0]	
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[7] M_DCLKA1	AU25	SA_CK[1]	
[7] M_DCLKA2	AW27	SA_CK[2]	
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[7] M_DCLKA3	AU26	SA_CK[3]	
[7] M_DCLKA3	AW26	SA_CK[3]	
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	AV12	SA_DQS[8]	
	AU12	SA_ECC_CB[0]	
	AU14	SA_ECC_CB[1]	
	AW13	SA_ECC_CB[2]	
	AY13	SA_ECC_CB[3]	
	AU13	SA_ECC_CB[4]	
	AY12	SA_ECC_CB[5]	
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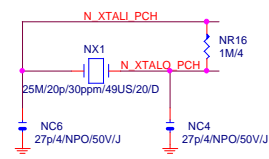






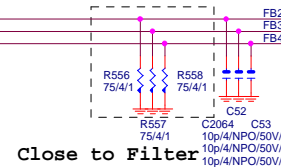
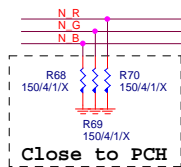
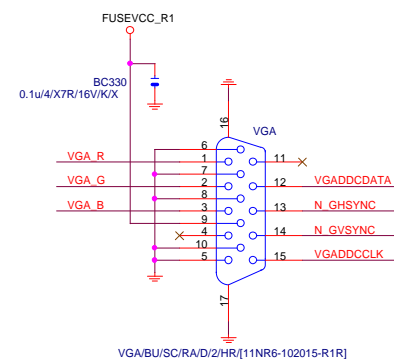
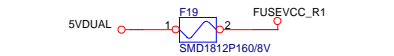
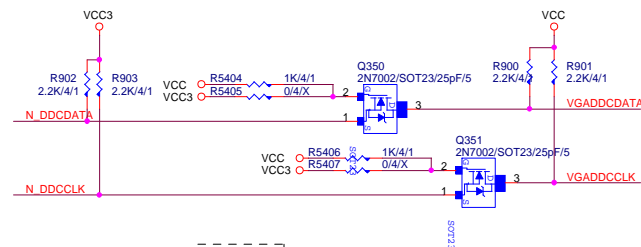
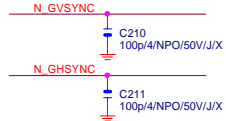
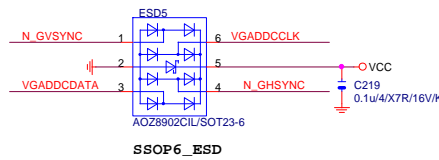
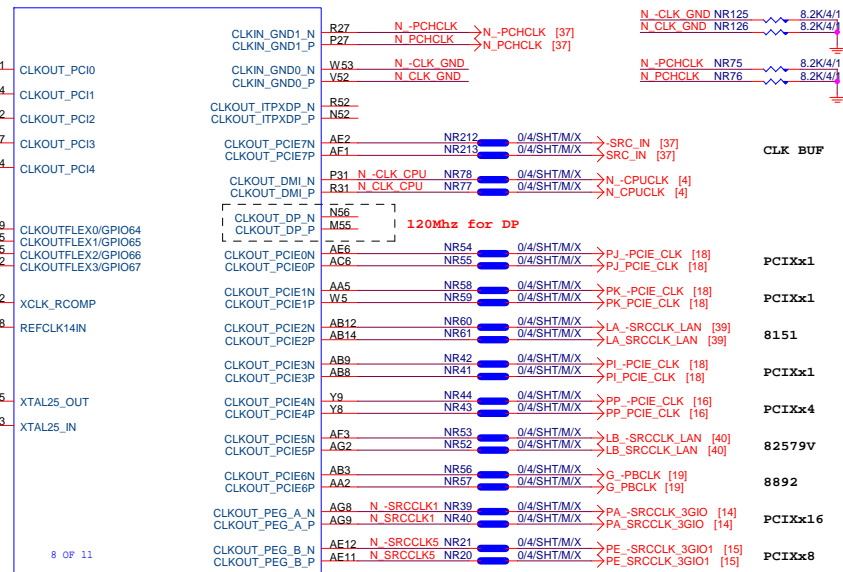


Flex0,2 : 33MHZ
 Flex1,3 : 27/14/24/48/25MHZ



N_PCHCLK14 NR33 8.2K/4/1

Mount for integrated clock Generation Mode



Gigabyte Technology			
Title			
PCH DISPLAY ,CLK BUFFER			
Size	Document Number		Rev
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SATA:20/7.5/4.5/7.5/20 (breakout min 8/4/4/8)
Impedance=90 +/- 17.5%

PCHC

For WIFI

BA50

BF50

BF49

NR177

0/4/SHT/MX

N ME PWROK

NC19

0.01u/4/X7R/25V/K/X

N GPIO17

N GPIO1

N GPIO6

N PHASE_CTRL

N GPIO68

N GPIO69

N GPIO70

N GPIO71

[34] N_SSTCTL

NC43

CL_CLK1

CL_DATA1

CL_RST1#

APWROK

PWM0

PWM1

PWM2

PWM3

TACH0/GPIO17

TACH1/GPIO1

TACH2/GPIO6

TACH3/GPIO7

TACH4_GPIO68

TACH5_GPIO69

TACH6_GPIO70

TACH7_GPIO71

SST

SCLOCK/GPIO22

SLOAD/GPIO38

SDATAOUT0/GPIO39

SDATAOUT1/GPIO48

NC_5

AY20

NRN8

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

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N GPIO70

N GPIO17

N GPIO1

N -PIROG

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N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

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N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

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N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

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N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

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N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

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N PHASE_CTRL

NRN7

8.2K/8P4R/4

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N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

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N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

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N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

N GPIO70

N GPIO17

N GPIO1

N -PIROG

N GPIO71

N GPIO68

N PHASE_CTRL

NRN7

8.2K/8P4R/4

N GPIO6

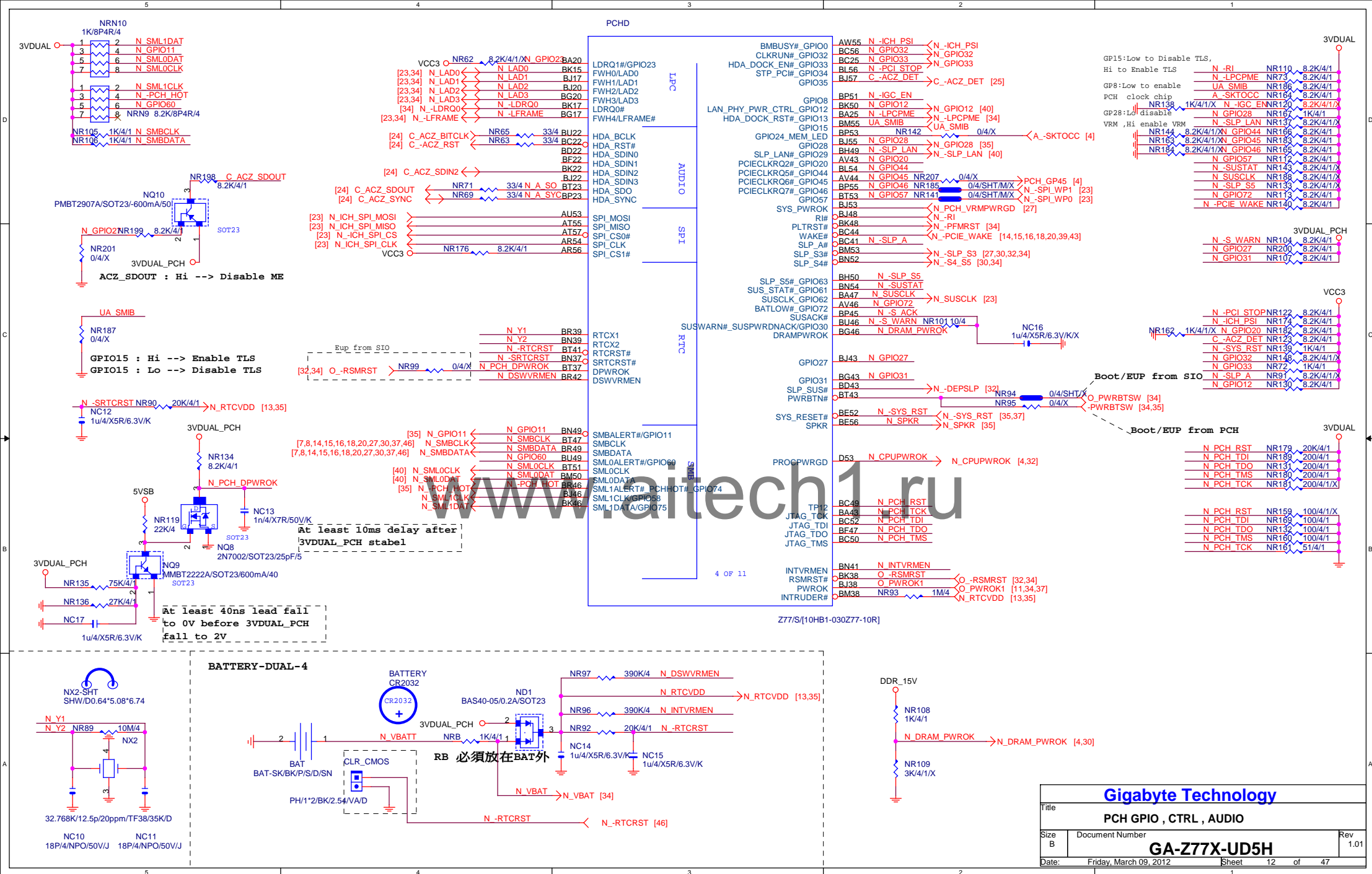
N GPIO70

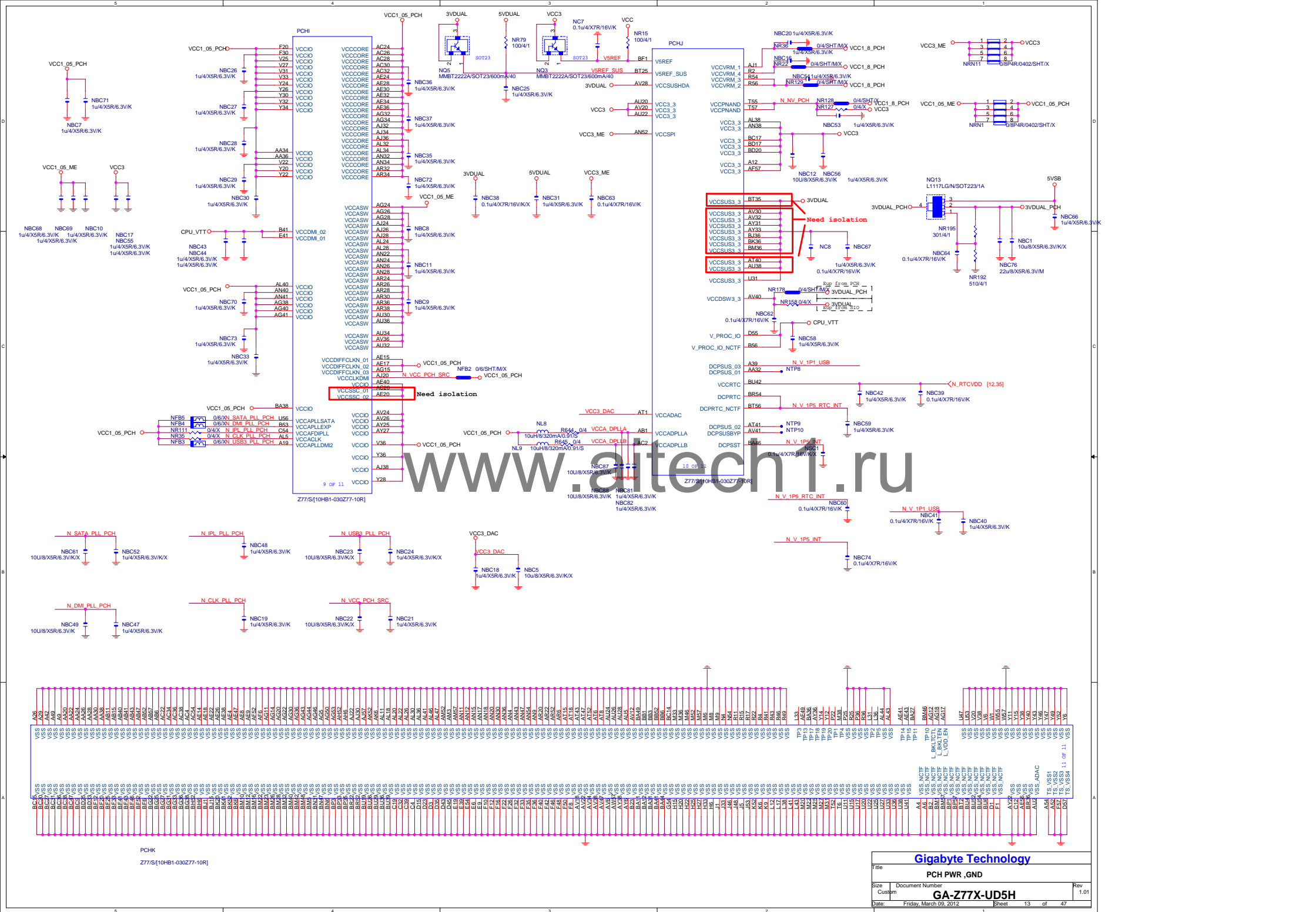
N GPIO17

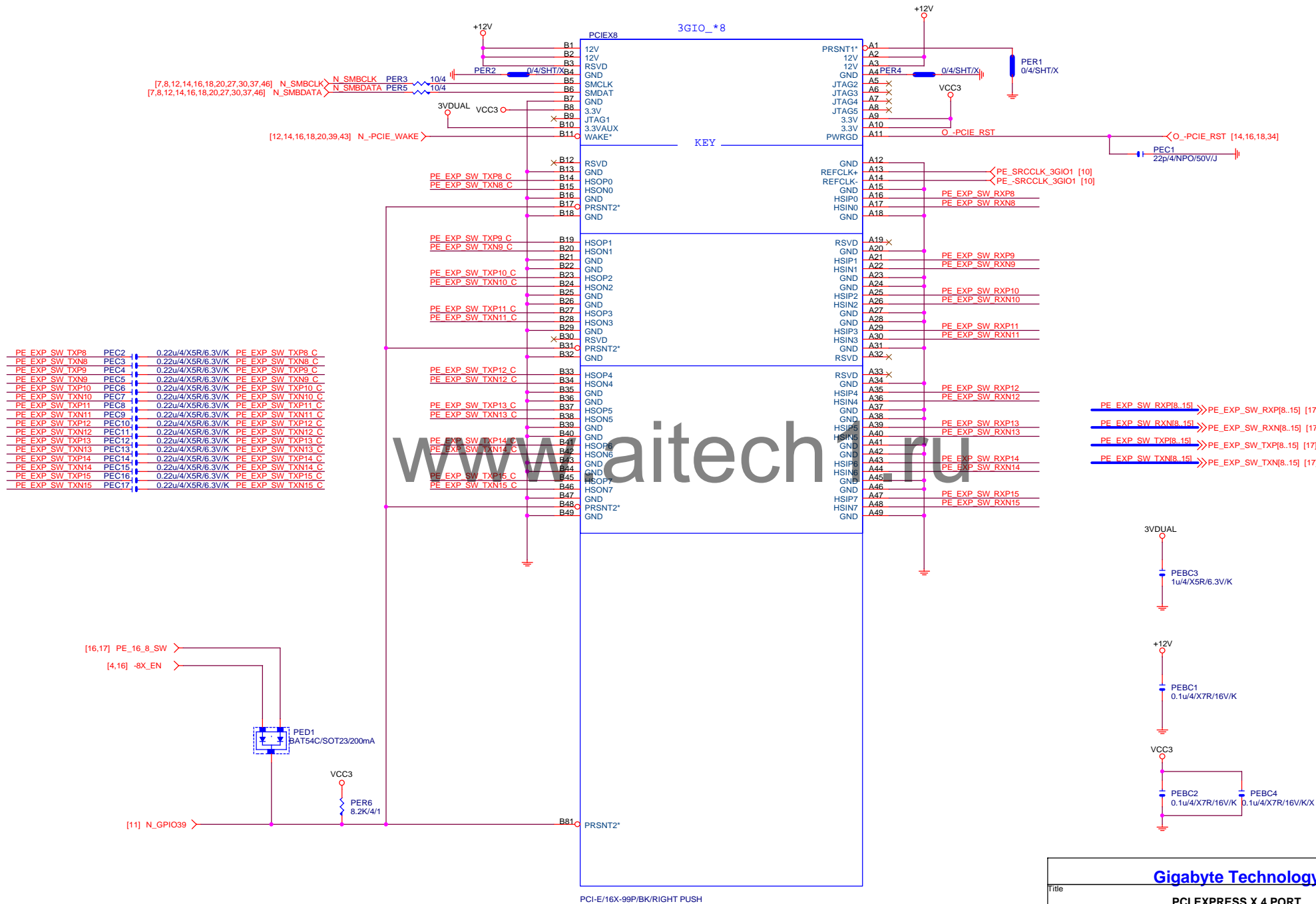
N GPIO1

N -PIROG

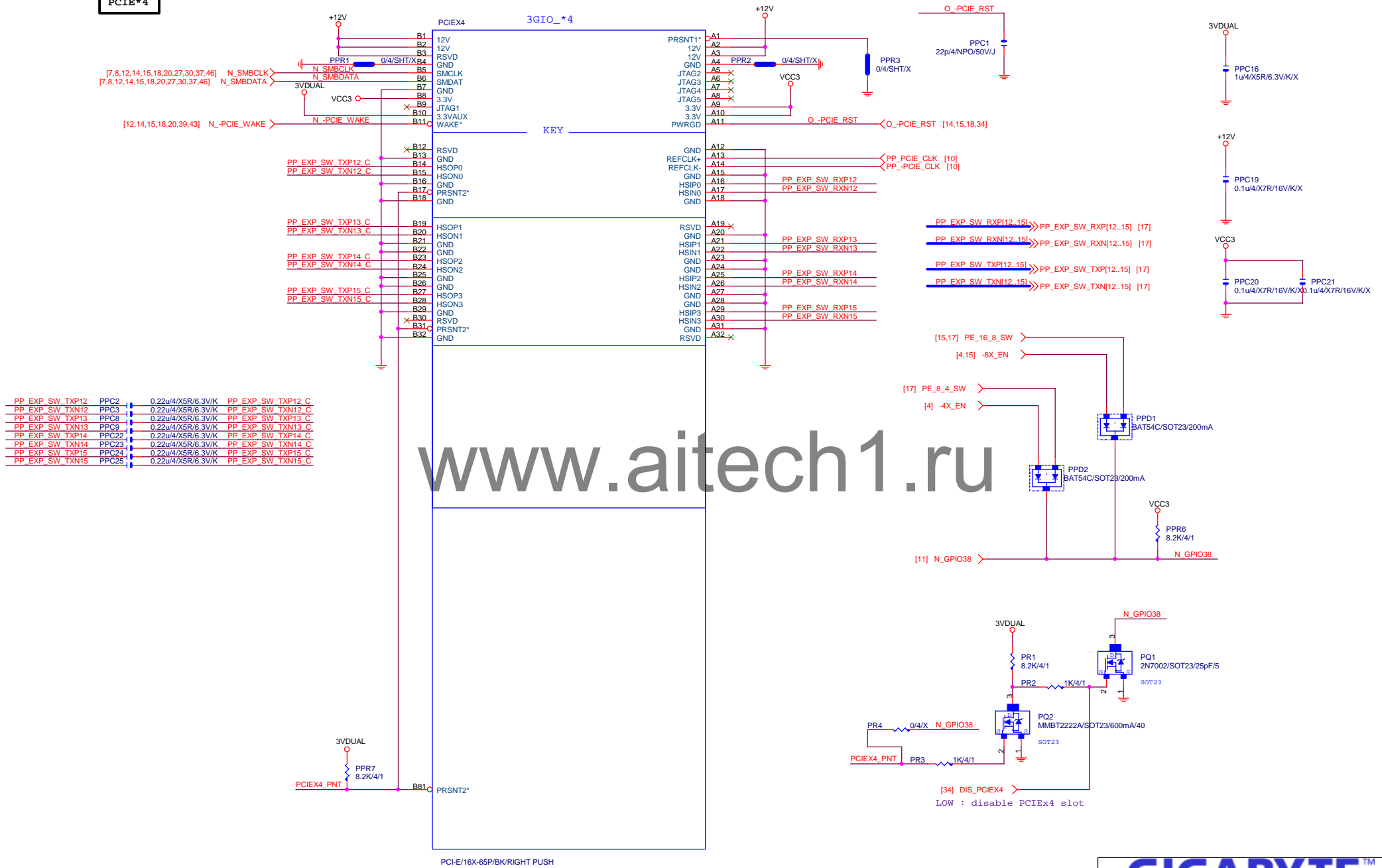
N GPIO71

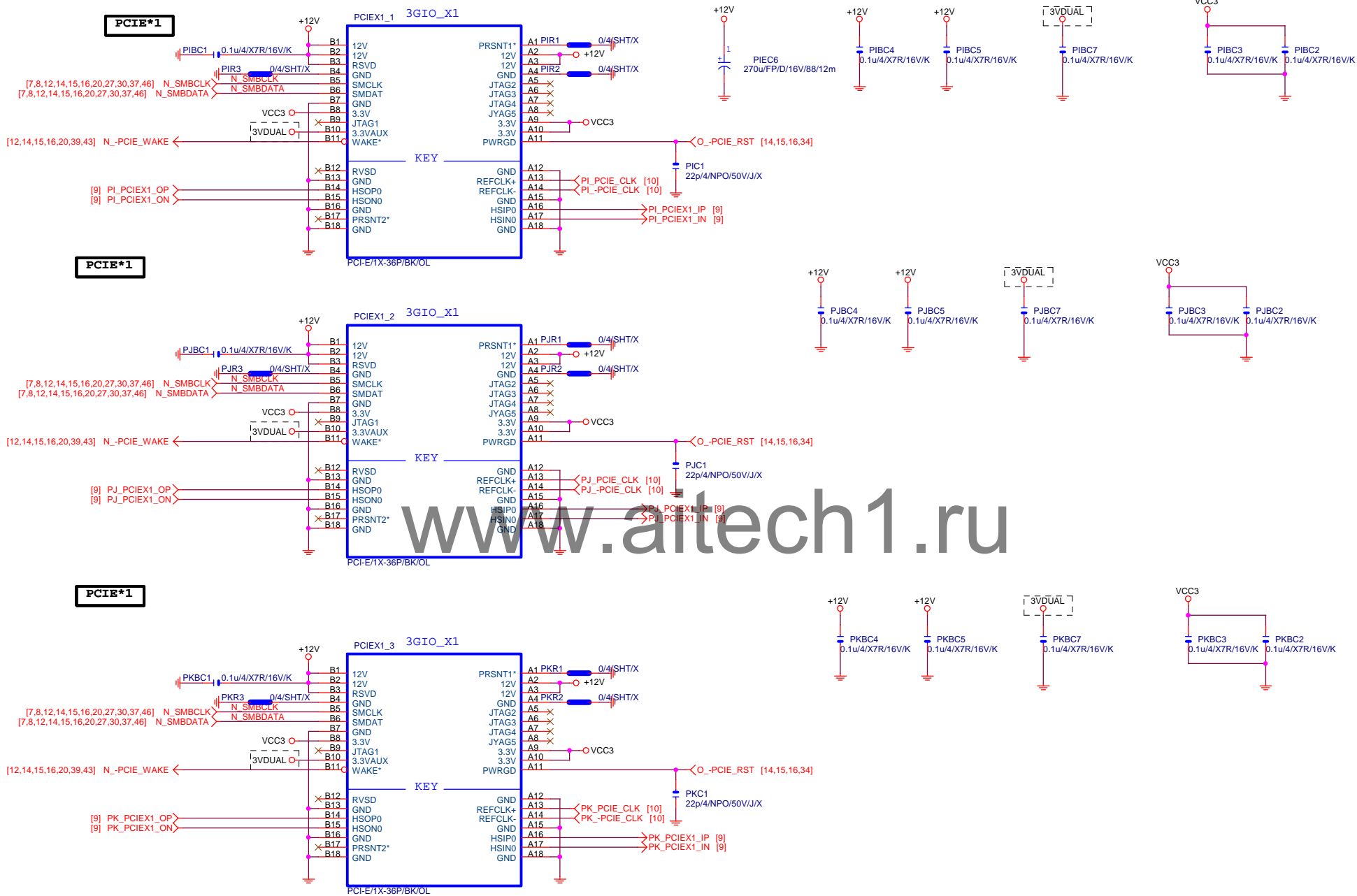






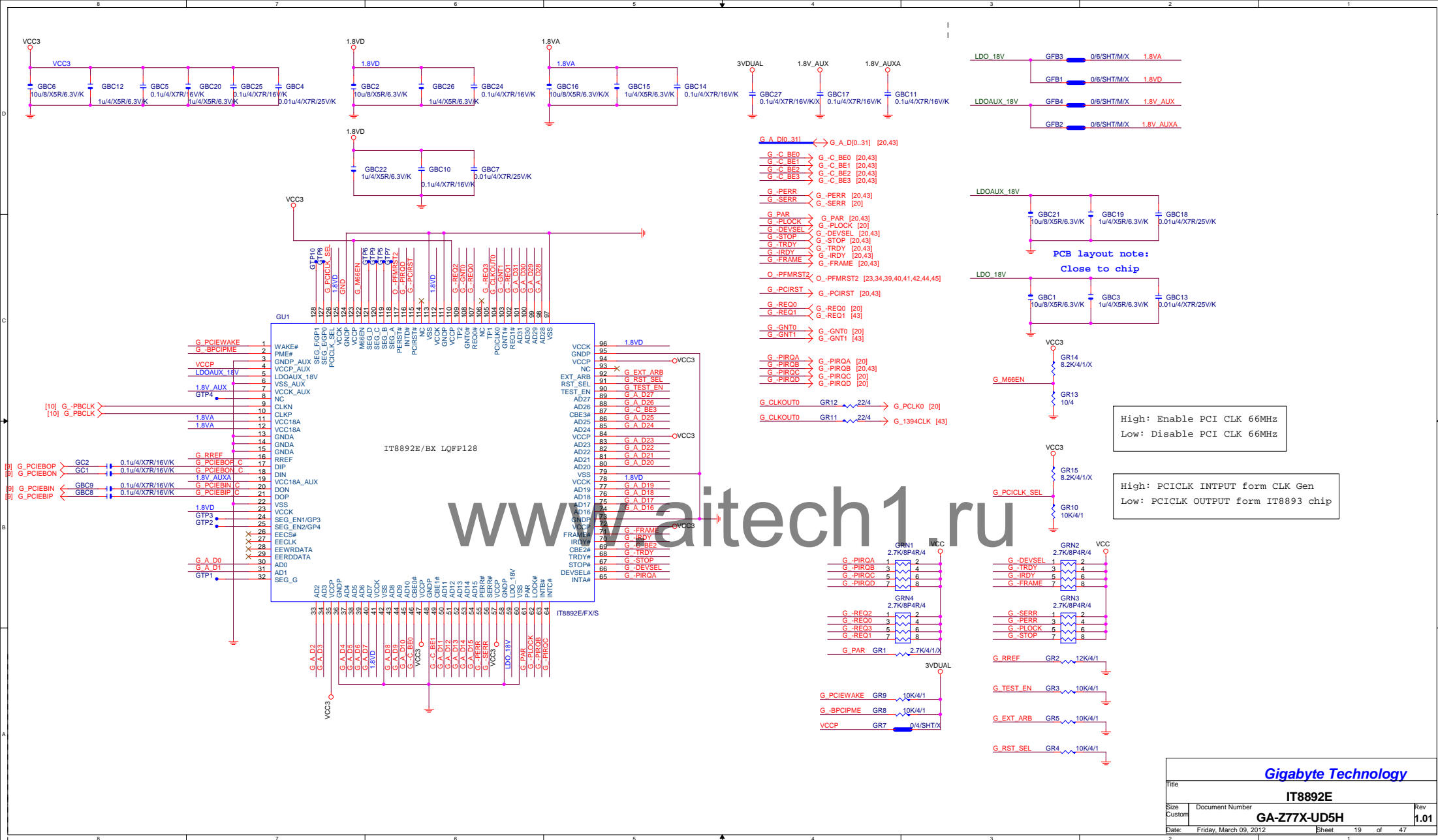
PCIE*4



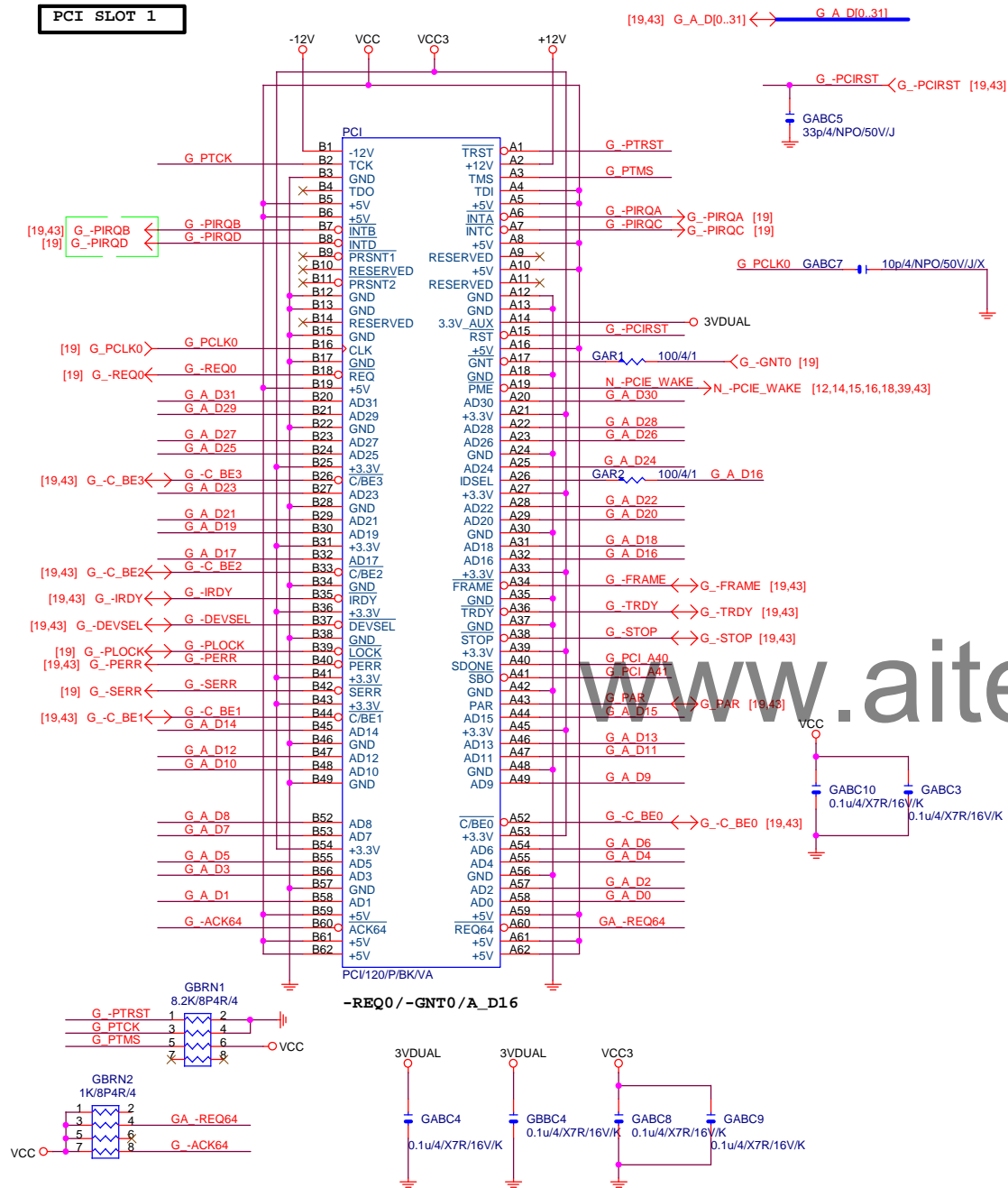


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Title		
PCIE_X1 1,2		
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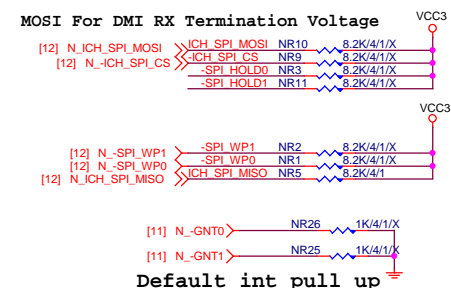
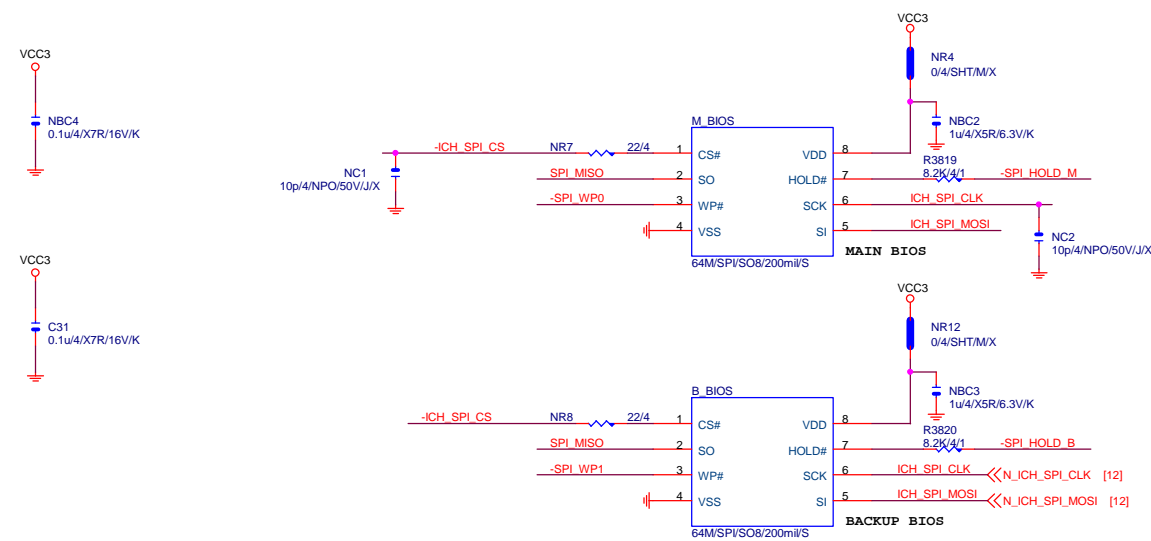


PCI SLOT 1



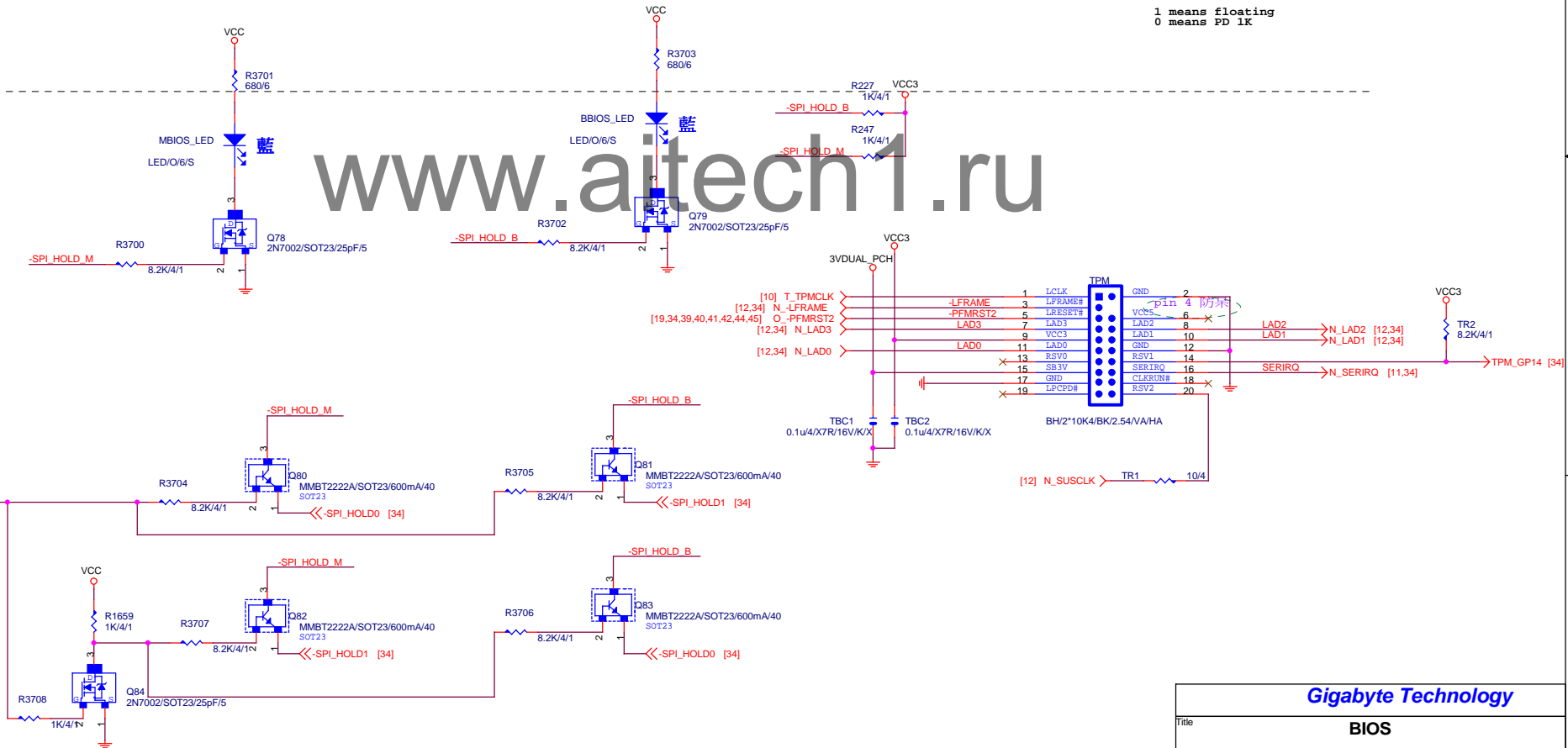
GIGABYTE™

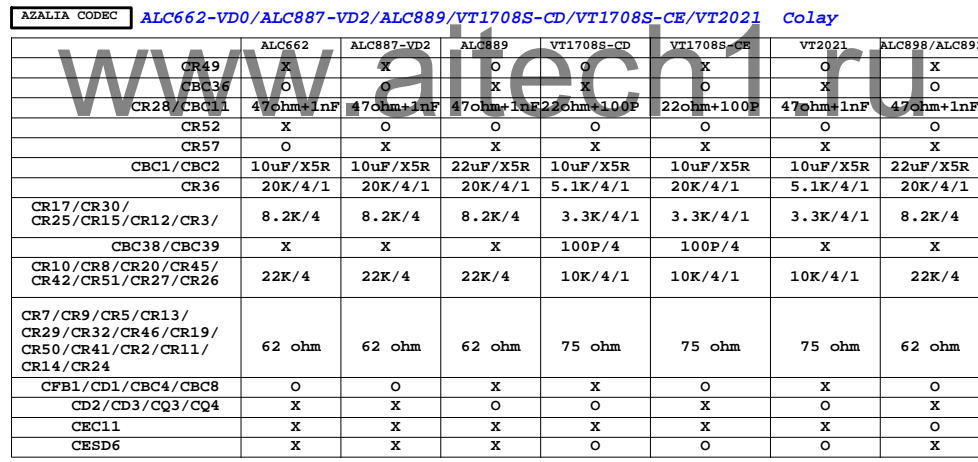
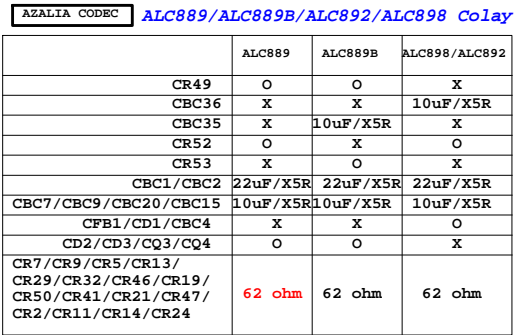
Title			
PCI SLOT 1&2			
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BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

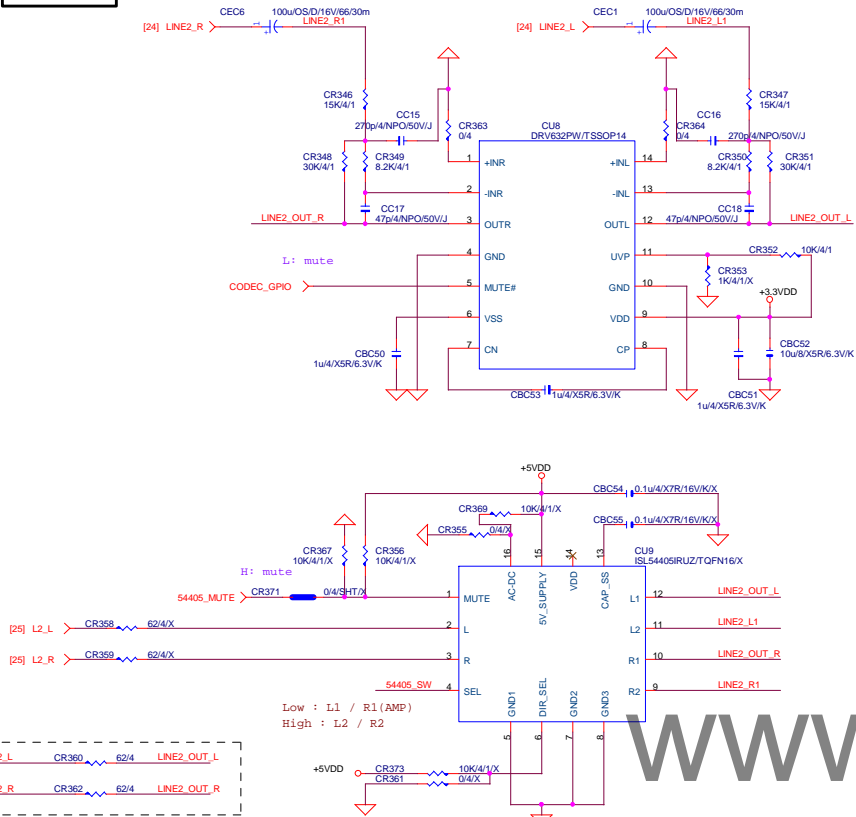
1 means floating
0 means PD 1K



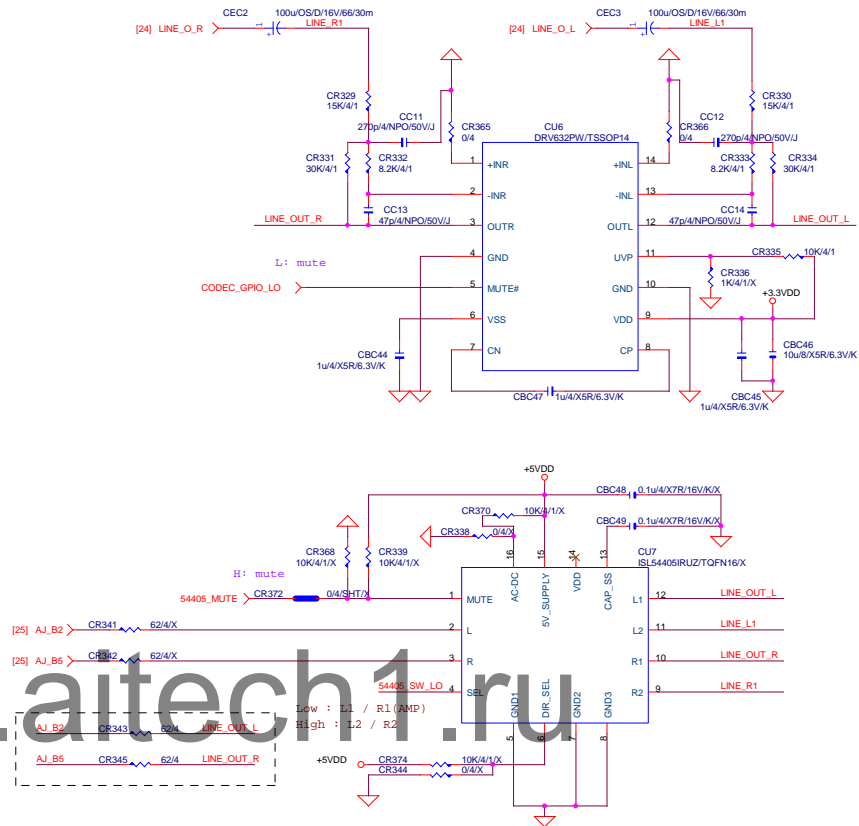


Gigabyte Technology			
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HEADPHONE



LINE-OUT



HEADPHONE

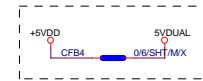
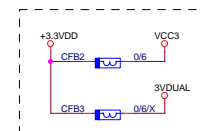
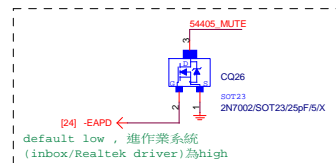
```

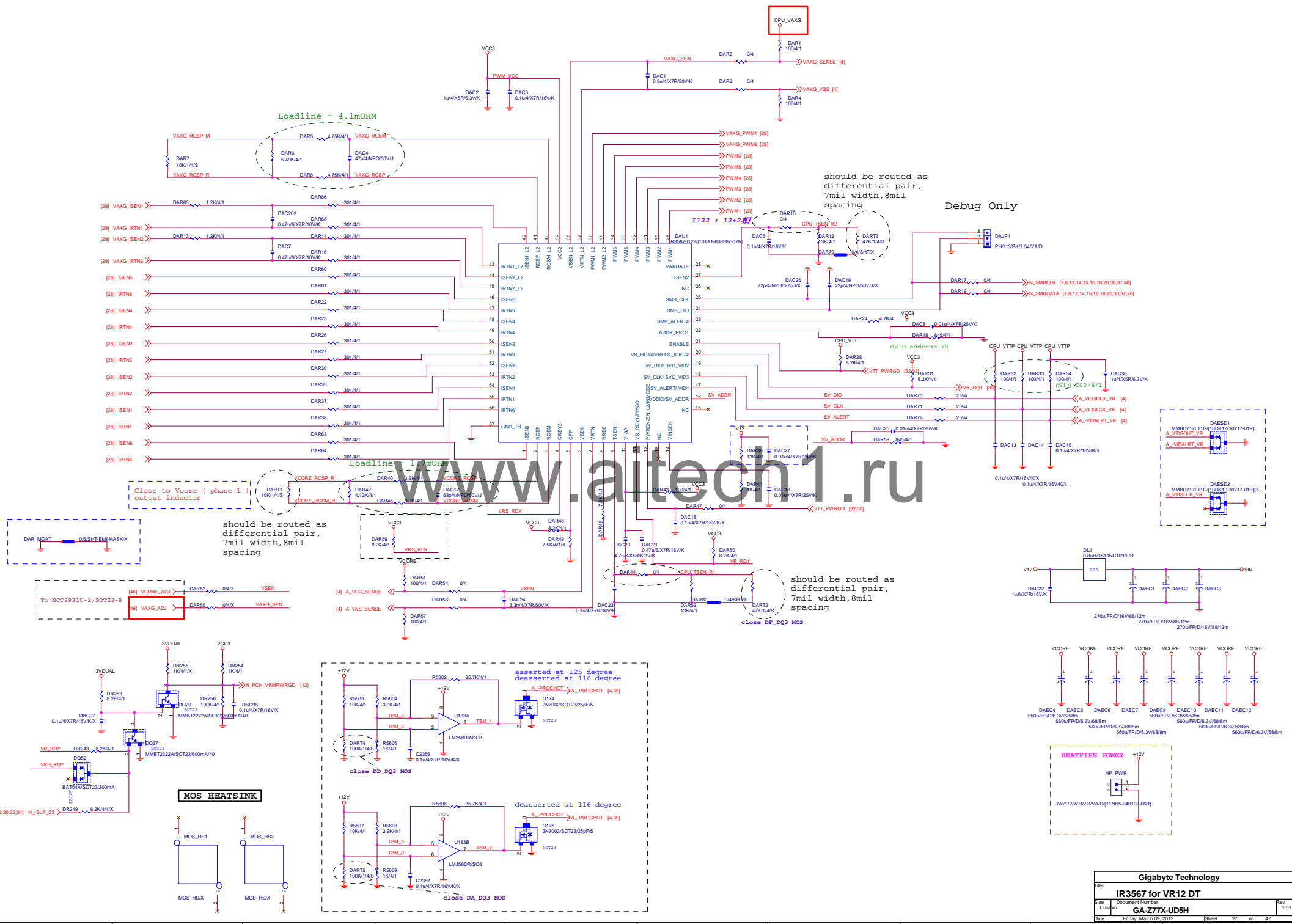
AMP_CODEC for 889
AMP_CODEC1 for 898/8
[24,25] AMP_CODEC ← CR25
[24] AMP_CODEC1 ← CR32
-----
LOW : NORMAL
HIGH : AMPLIFY
inbox driver default low
Realtek driver 為 high

```

LINE-OUT

```
LOW : NORMAL
HIGH : AMPLIFY
inbox driver default low
Realtek driver 為 high
```





[illegible]

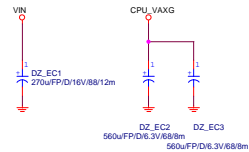
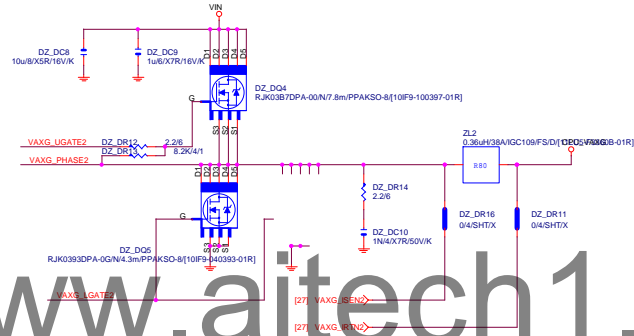
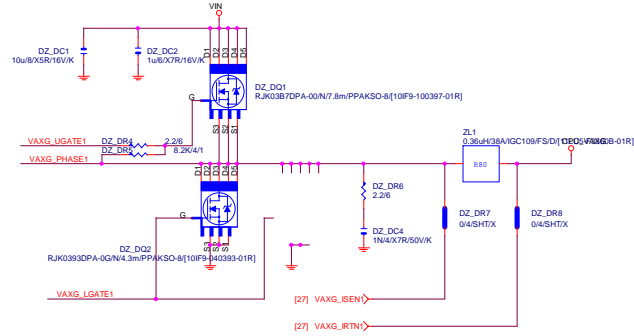
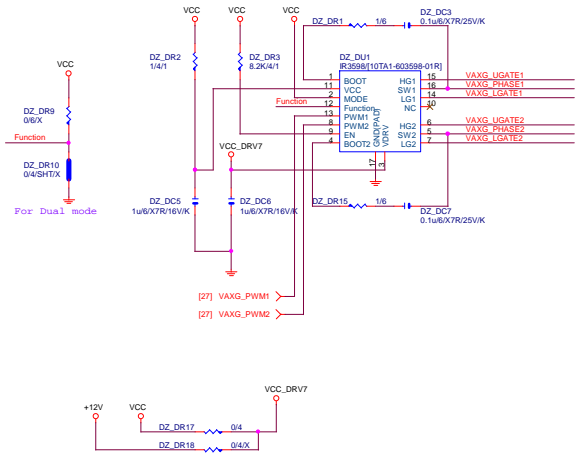
The schematic diagram illustrates the 128-bit AES encryption algorithm. It starts with a master key (KEY) and a counter (COUNT) to generate a Key Schedule. The Key Schedule produces round keys (KEY1 to KEY10) and an inverse key (KEY11). The encryption process begins with an initial AddRoundKey operation using KEY1. The main encryption loop consists of 10 rounds, each containing a SubBytes operation, a ShiftRows operation, a MixColumns operation, and an AddRoundKey operation using the corresponding round key. The final output is the encrypted data (ENCRYPTED DATA), which is then decrypted using the inverse key (KEY11) and the inverse ShiftRows operation to produce the original data (DATA).

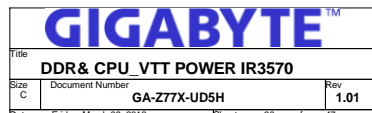


The schematic diagram illustrates the digital logic circuit for the 4-bit adder. It consists of the following components and connections:

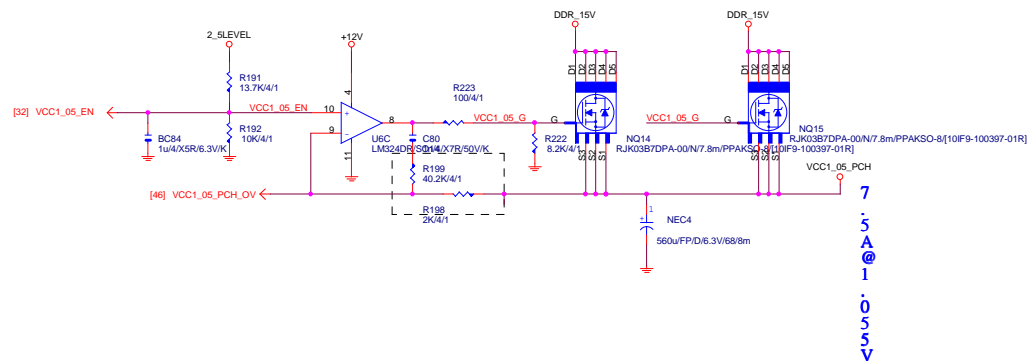
- 74LS161 4-bit binary counters:** Two counters are used. The first counter (top) has its \overline{EN} pin connected to VCC, its \overline{CLK} pin connected to a 10 kHz square wave, and its \overline{EN} pin connected to the output of the first 74LS148 decoder. The second counter (bottom) has its \overline{EN} pin connected to VCC, its \overline{CLK} pin connected to a 10 kHz square wave, and its \overline{EN} pin connected to the output of the second 74LS148 decoder.
- 74LS148 3-to-8 line decoders:** Two decoders are used. The first decoder (top) has its \overline{EN} pin connected to VCC, its \overline{CLK} pin connected to a 10 kHz square wave, and its \overline{EN} pin connected to the output of the first 74LS161 counter. The second decoder (bottom) has its \overline{EN} pin connected to VCC, its \overline{CLK} pin connected to a 10 kHz square wave, and its \overline{EN} pin connected to the output of the second 74LS161 counter.
- 74LS160 4-bit binary counter:** A single counter is used. Its \overline{EN} pin is connected to VCC, its \overline{CLK} pin is connected to a 10 kHz square wave, and its \overline{EN} pin is connected to the output of the second 74LS148 decoder. The output of the 74LS160 counter is connected to the output of the second 74LS161 counter.
- Power and Ground:** The circuit is powered by VCC and GND. The VCC pin of the 74LS160 counter is connected to VCC, and its \overline{EN} pin is connected to GND. The GND pin of the 74LS160 counter is connected to GND.

VAXG Phase



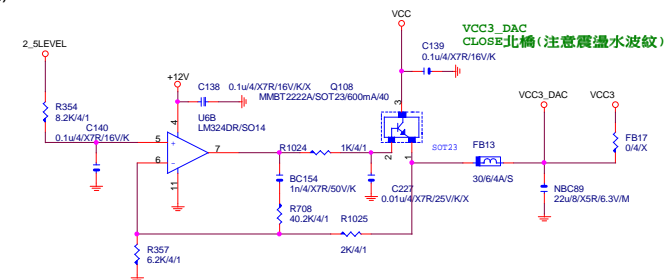


VCC1_05_PCH

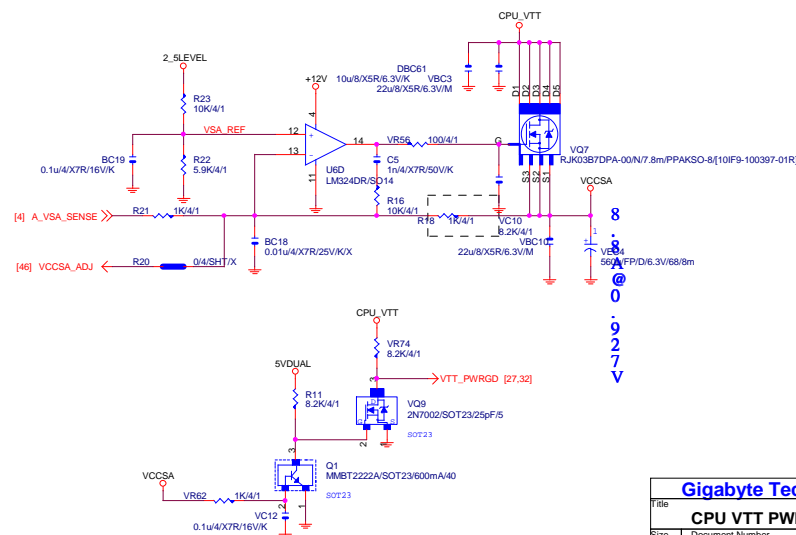
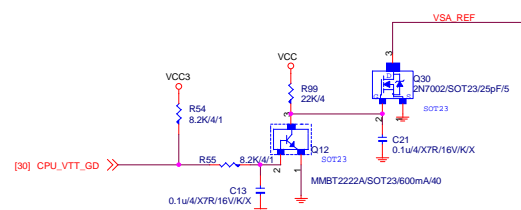


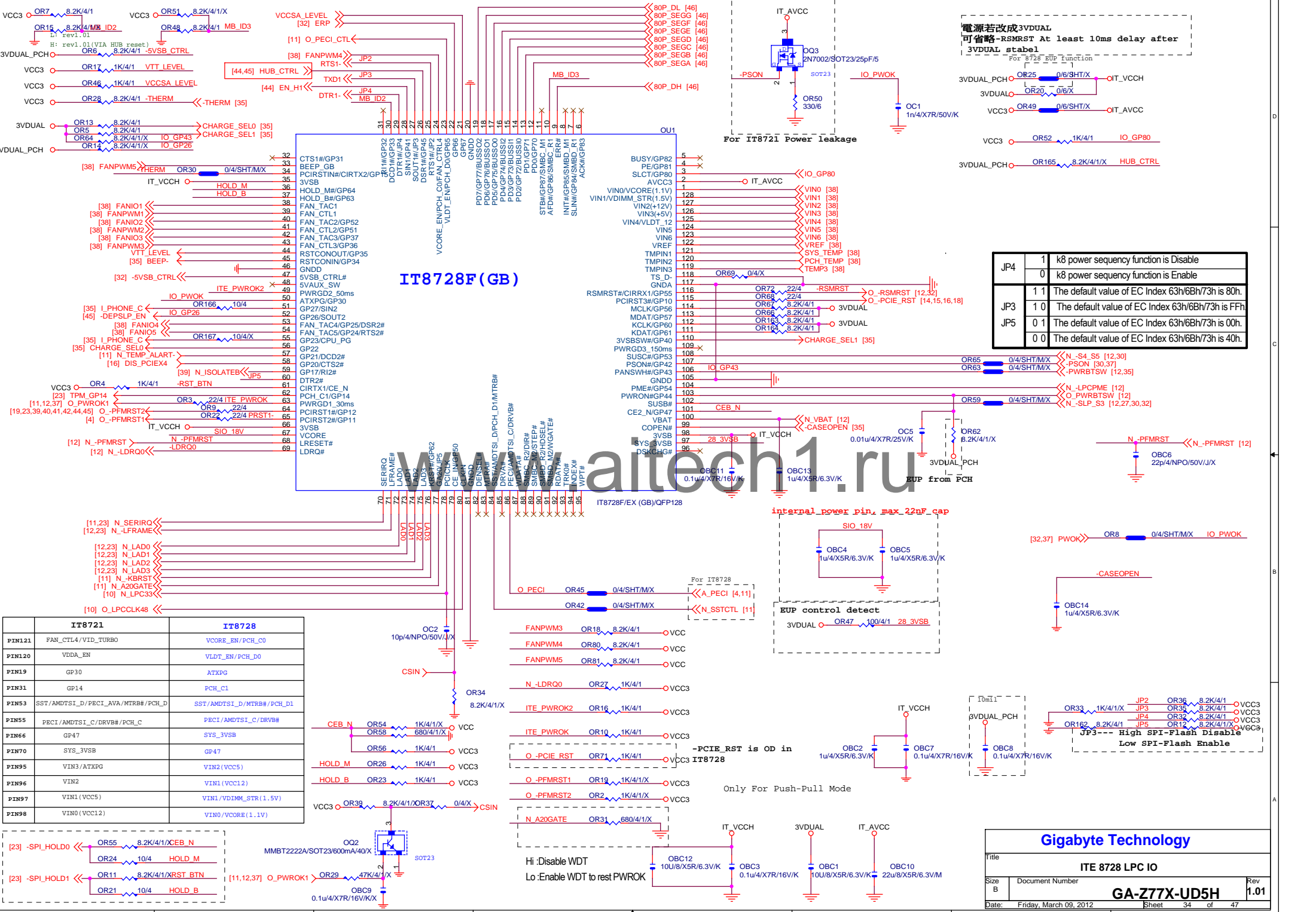
VCC3_DAC

(3.3V/70mA+360uA)



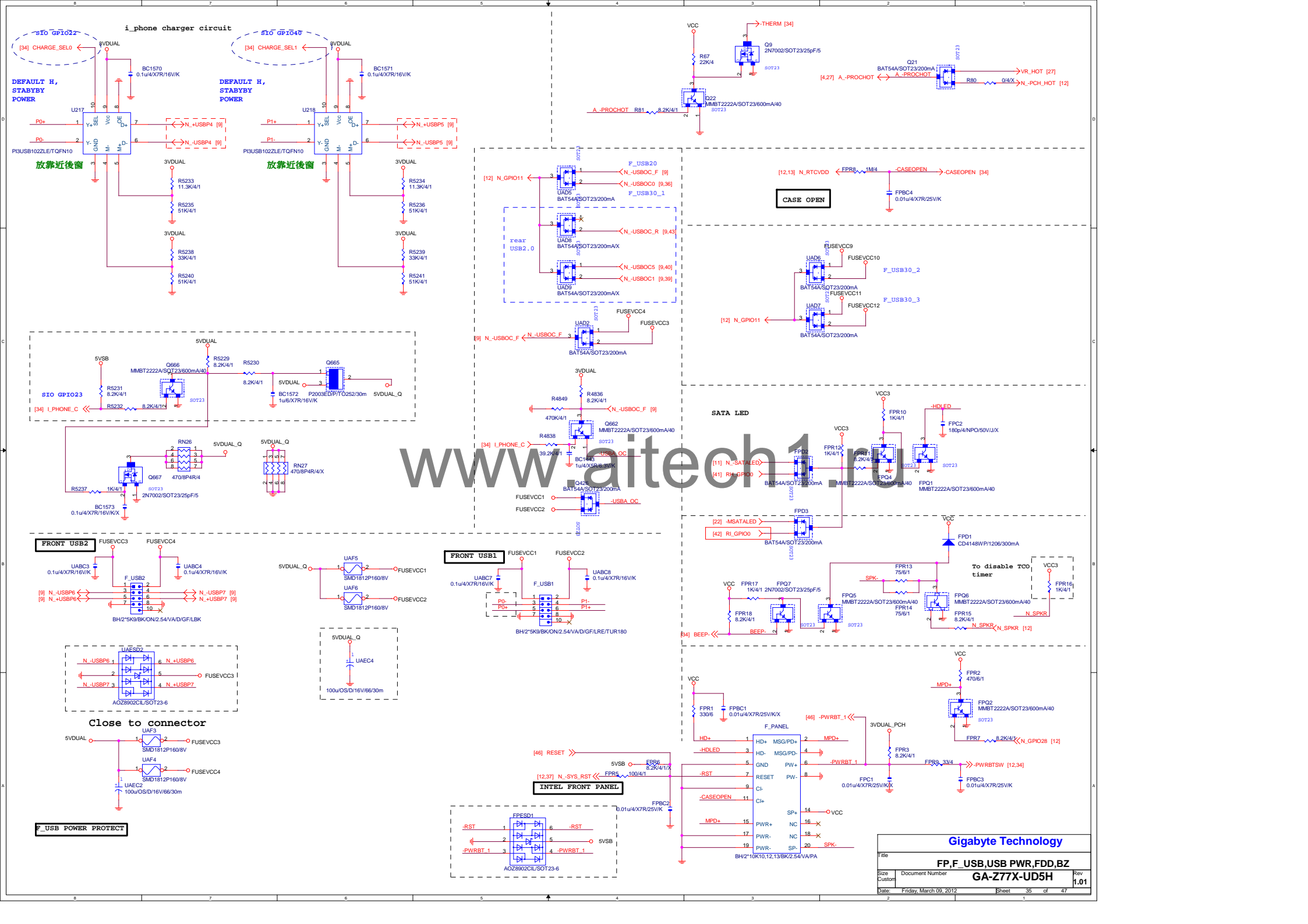
VCC_SA



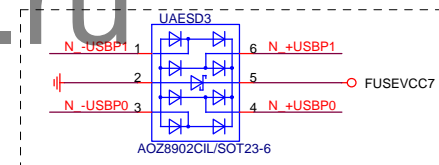
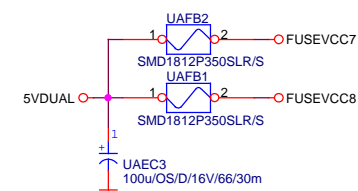
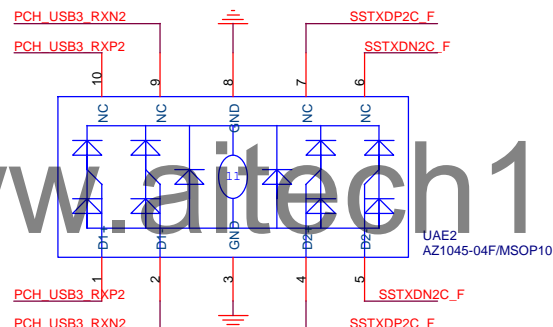
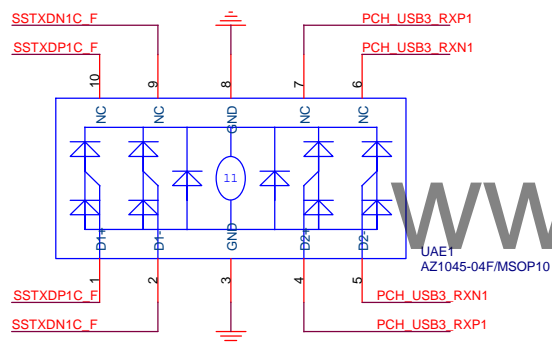
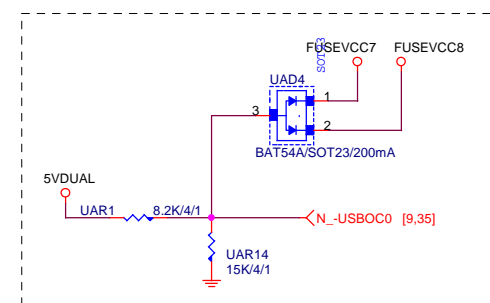
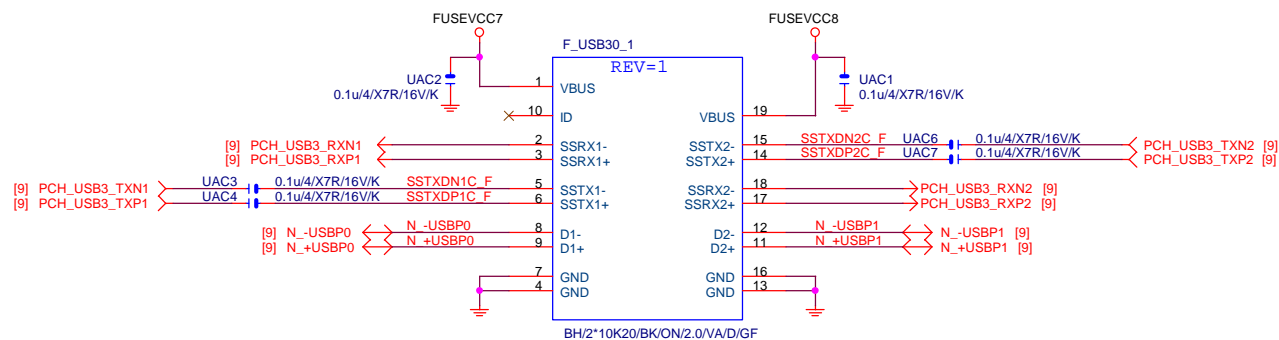


電源若改成3VDUAL
可省略-RSMRST At least 10ms delay after
3VDUAL stabl
For 3.26 SOT23 Function

JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

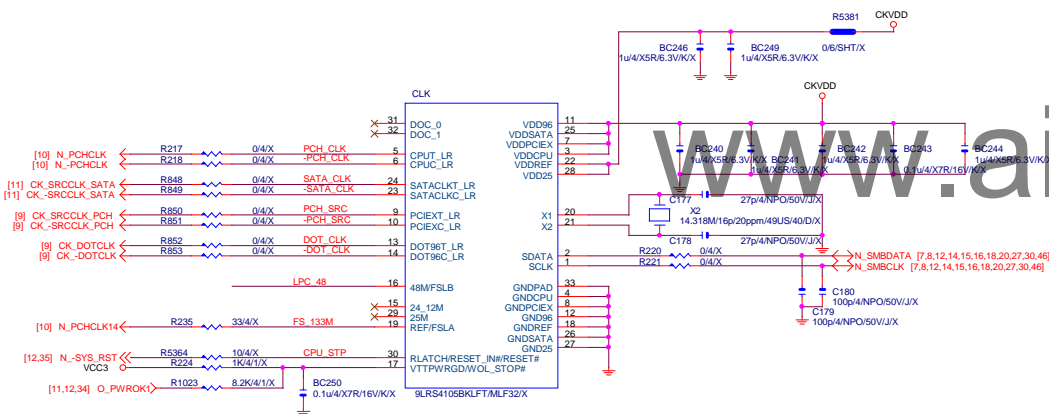
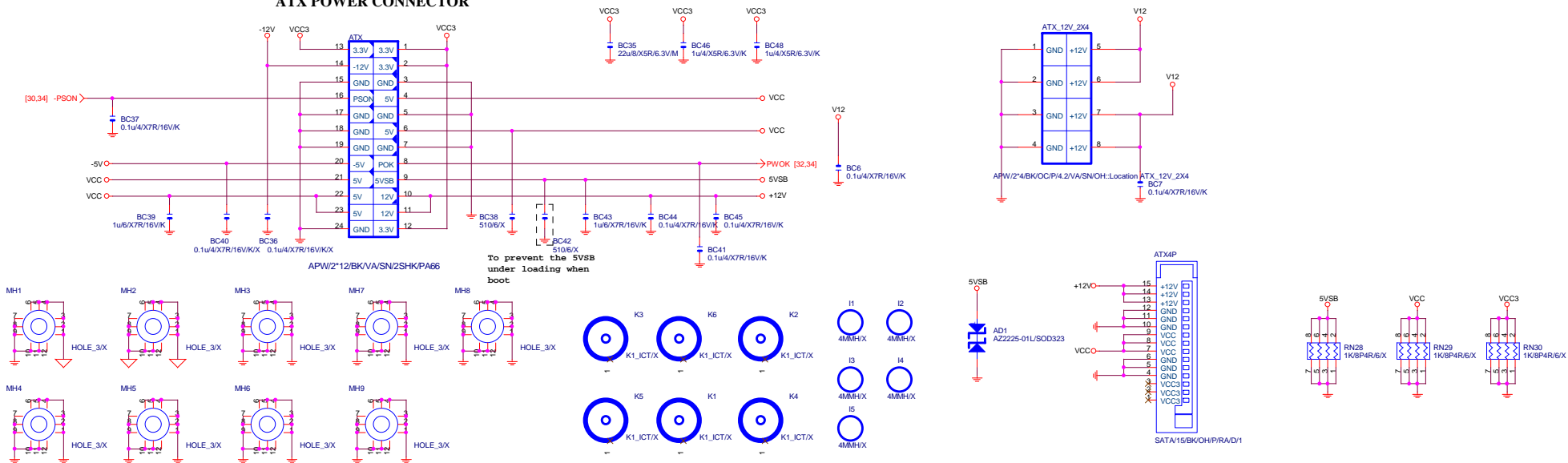


www.aitech1.com

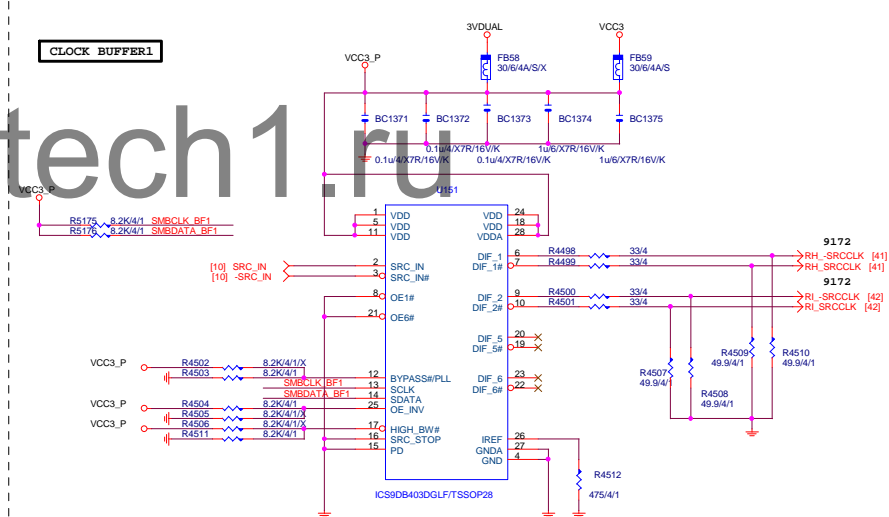


Gigabyte Technology			
Title			
FP,F_USB,USB PWR,FDD,BZ			
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ATX POWER CONNECTOR



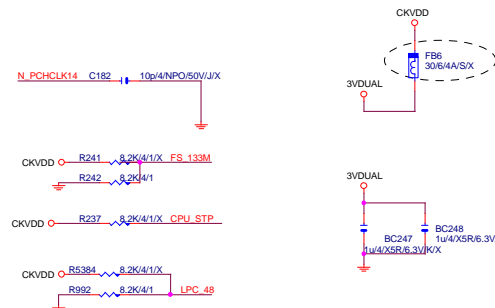
CLOCK BUFFER1



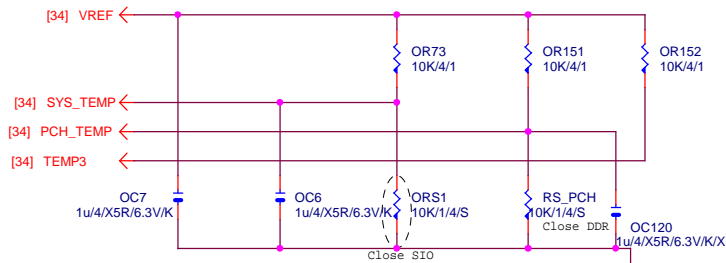
CLK GEN CK505

CPU Frequency Selection

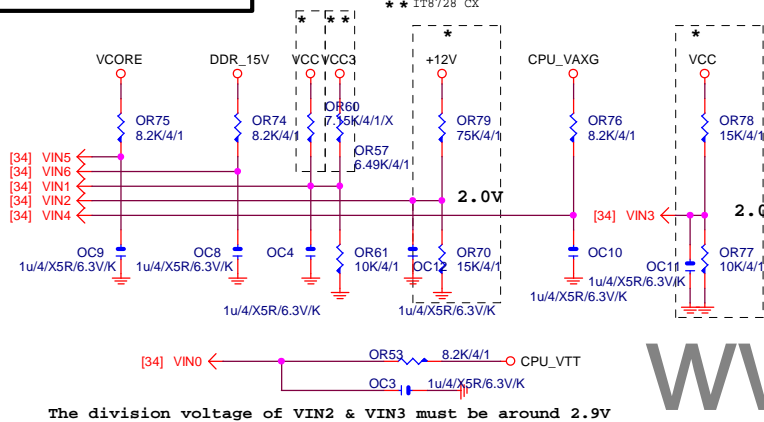
FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



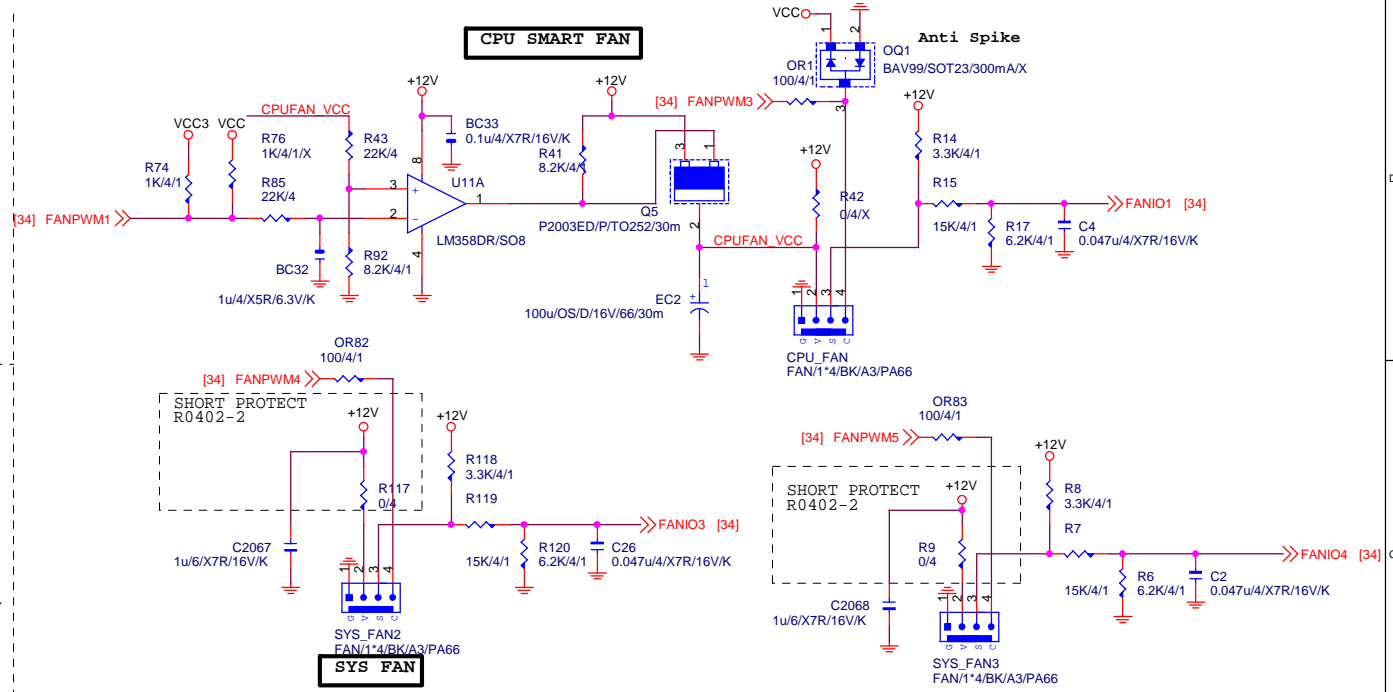
TEMP H/W MONITOR



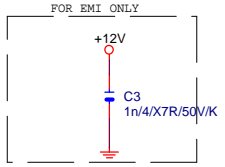
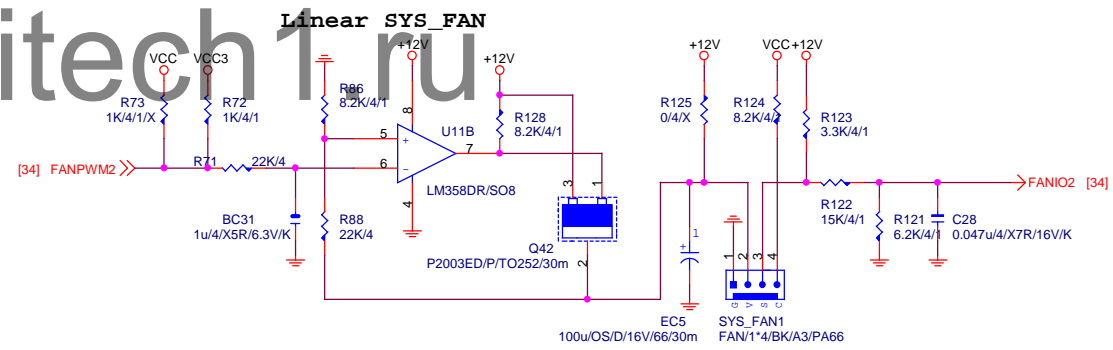
VOLTAGE-- H/W MONITOR



CPU SMART FAN

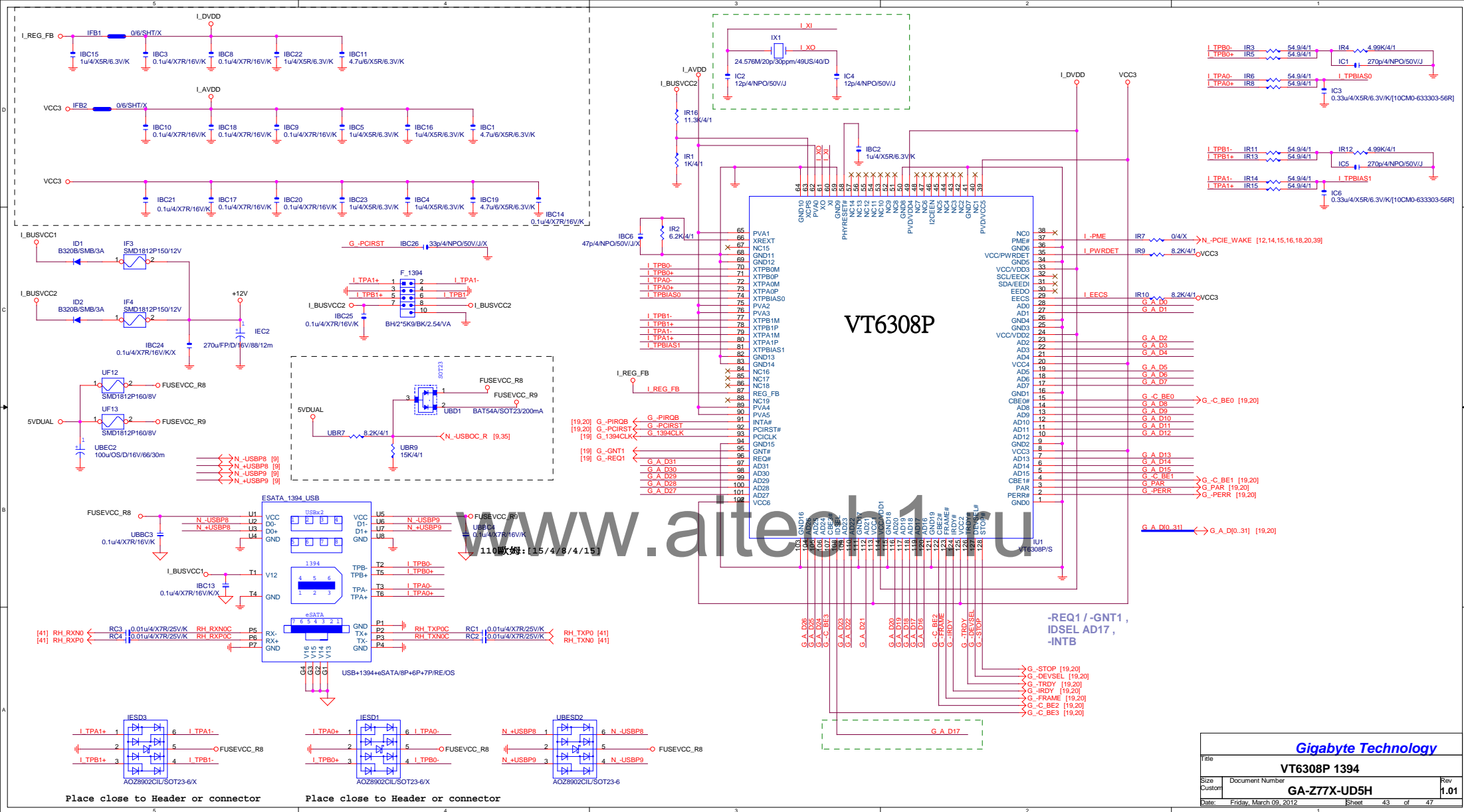


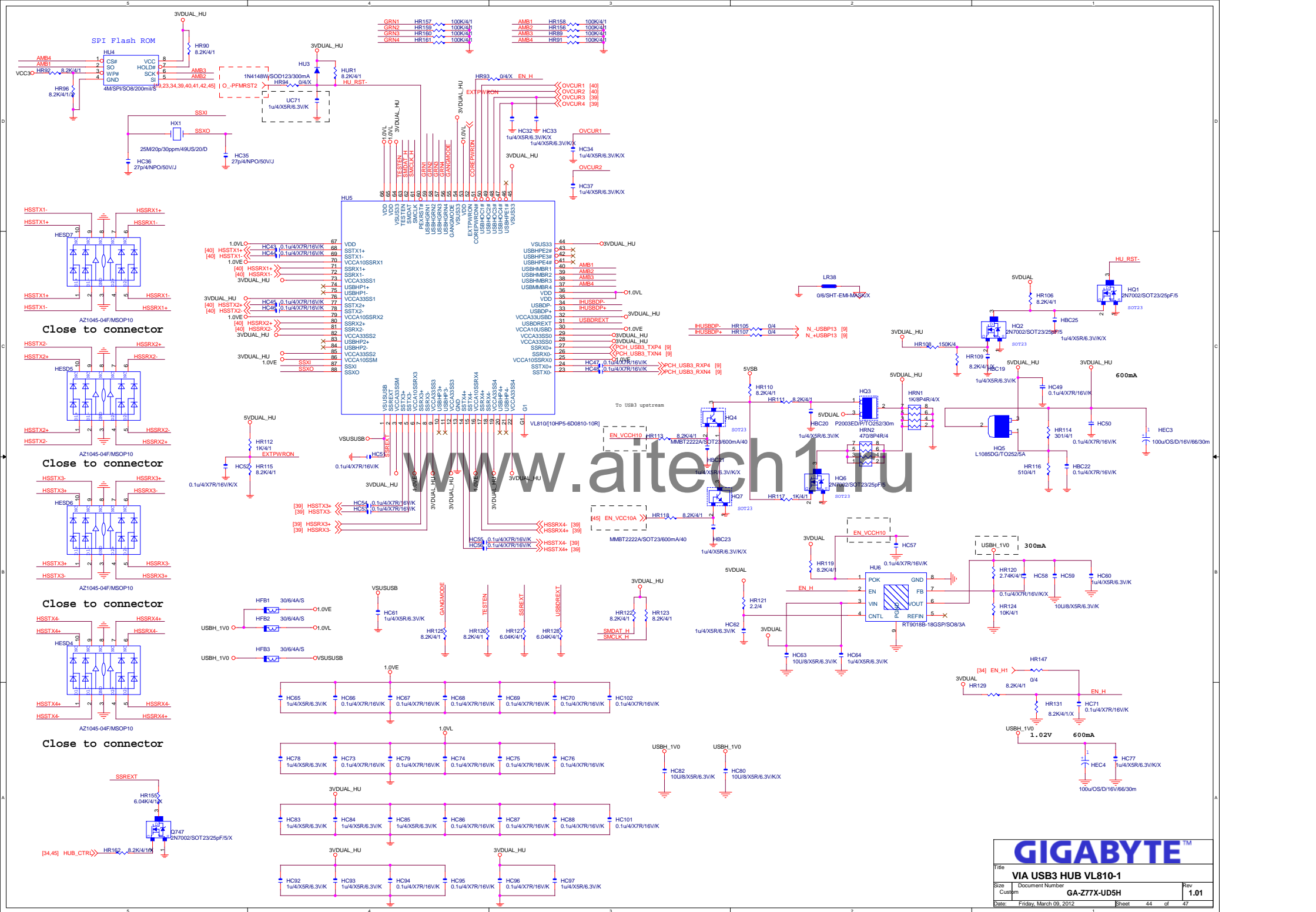
SYS FAN

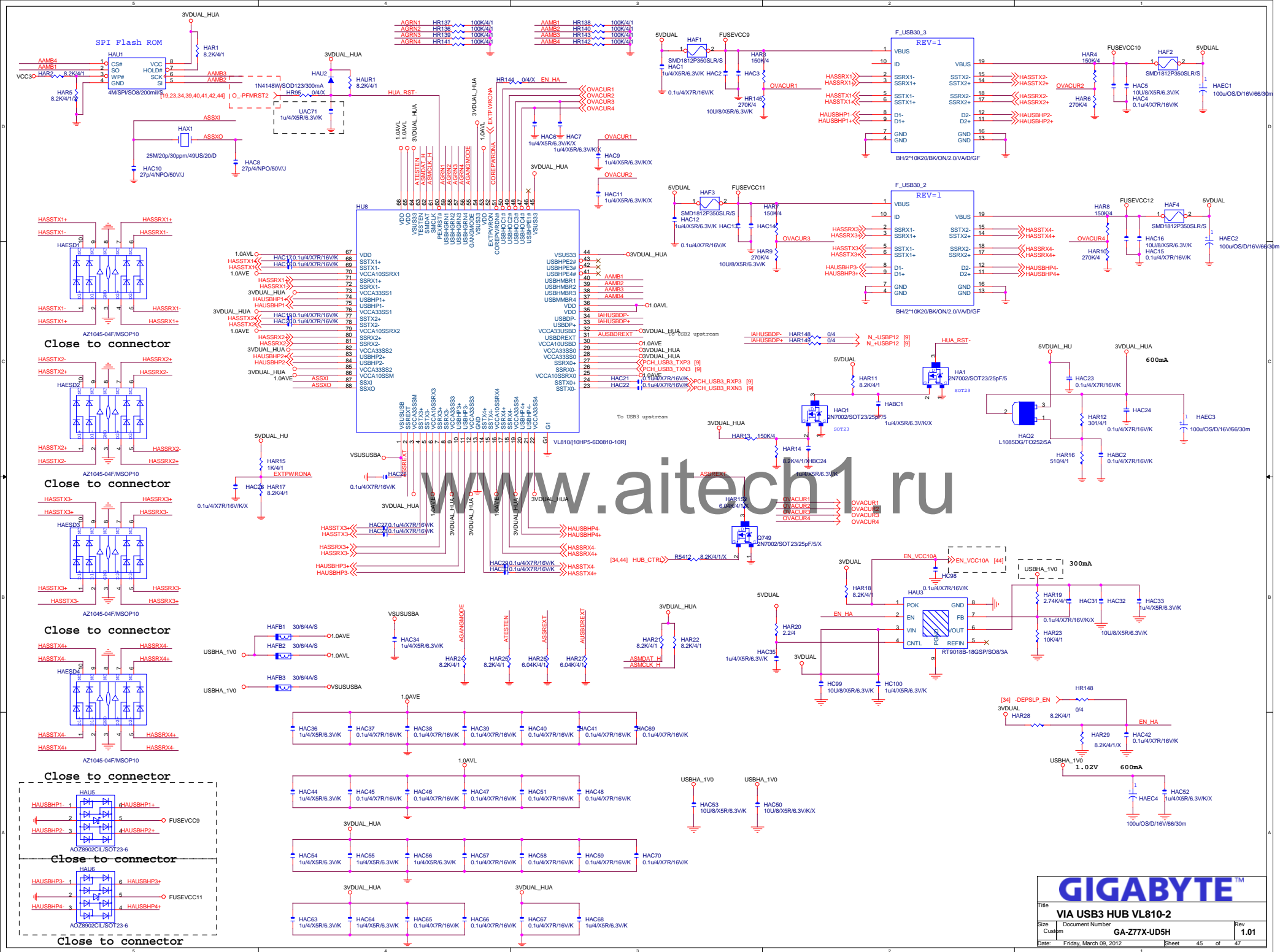


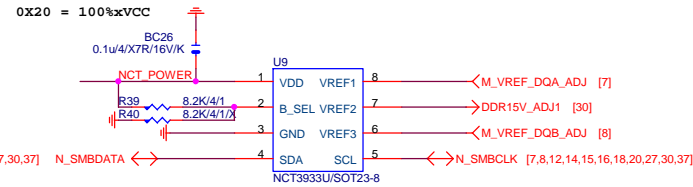
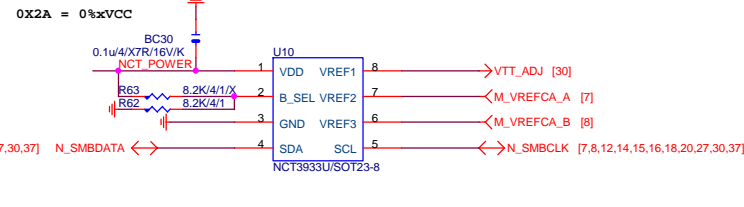
Gigabyte Technology

Title			
HWM,KB/MS, FAN CTRL			
Size	Document Number	Rev	
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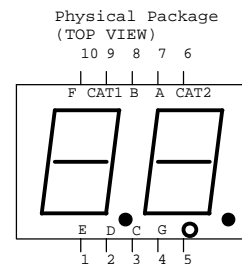
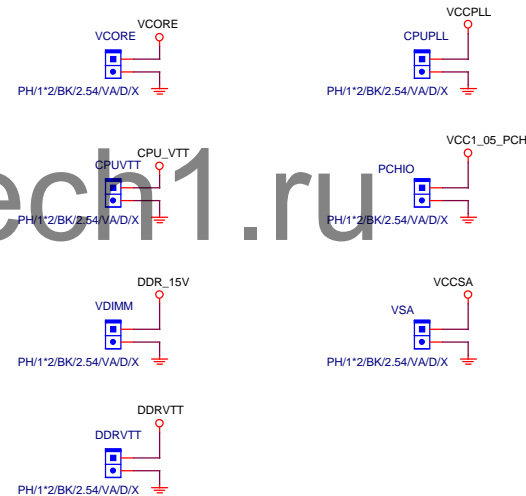








COMMON CATHODE

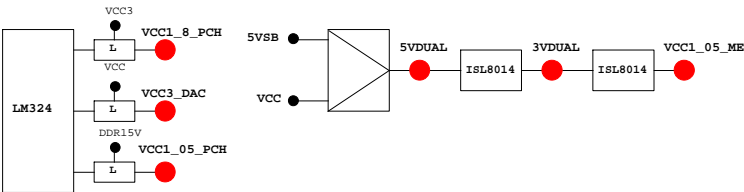


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQ#	MAIN		GPI -PIRQE	P/U 8.2K VCC3	
GP3/PIRQ#	MAIN		GPI -PIRQF	P/U 8.2K VCC3	
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKT0CC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_FCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	

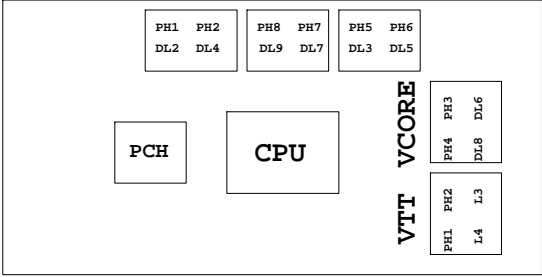
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PWRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBD_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBD_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
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